

CC065S
7.0 x 5.0 x 1.5 mm
LCC Ceramic Package

Features

- CMOS Output (will interface with TTL devices)
- Enable/Disable Function includes low standby power
- Low Jitter
- 5.0V nominal Supply Voltage
- 1-60 MHz Frequency Range

Applications

Driving A/Ds, D/As, FPGAs
Digital Video
Ethernet, GbE
Medical
Storage Area Networking
COTS
Broad Band Access
SONET/ SDH/ DWDM
Base Stations/ Picocell
Test & Measurement

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range ²	1	-	60	MHz	
Frequency Stability ²	±50	-	±100	ppm	Includes supply voltage change, load change, aging for 1 year at 25°C ± 2°C, shock, vibration and temperatures
Operating Temperature Range ²	0 -40	- -	+70 +85	°C	
Supply Voltage ^{1,2} V _{CC}	4.5	5.0	5.5	V	5.0V ± 10%
Input Current I _{CC}	- -	- -	25 35	mA	1 MHz ≤ F _o < 32 MHz 32 MHz ≤ F _o ≤ 60 MHz
Output Waveform	CMOS				CL = 15pF max
Duty Cycle	45	-	55	%	At 50% point of V _{CC}
Output V _{HIGH} V _{OH}	0.9V _{CC}	-	-	V	See Load Circuit
Output V _{LOW} V _{OL}	-	-	0.1V _{CC}	V	
Rise/Fall Time	-	-	10	ns	0.1V _{CC} ~ 0.9V _{CC} levels
Startup Time	-	-	10	ms	Time for output to reach specified frequency
V _{DISABLE} V _{IL}	-	-	0.3V _{CC}	V	applied to Pad 1
V _{ENABLE} V _{IH}	0.7V _{CC}	-	-		
Enable Time	-	-	10	ms	Time for output to reach a logic state
Disable Time	-	-	50	µs	Time for output to reach a high Z state
Enable/Disable Internal Pull-up	30	70	150	KΩ	To V _{CC}
Standby Current	-	-	10	µA	Pad 1 low, device disabled
Storage Temperature Range	-55	-	+125	°C	

Part Number

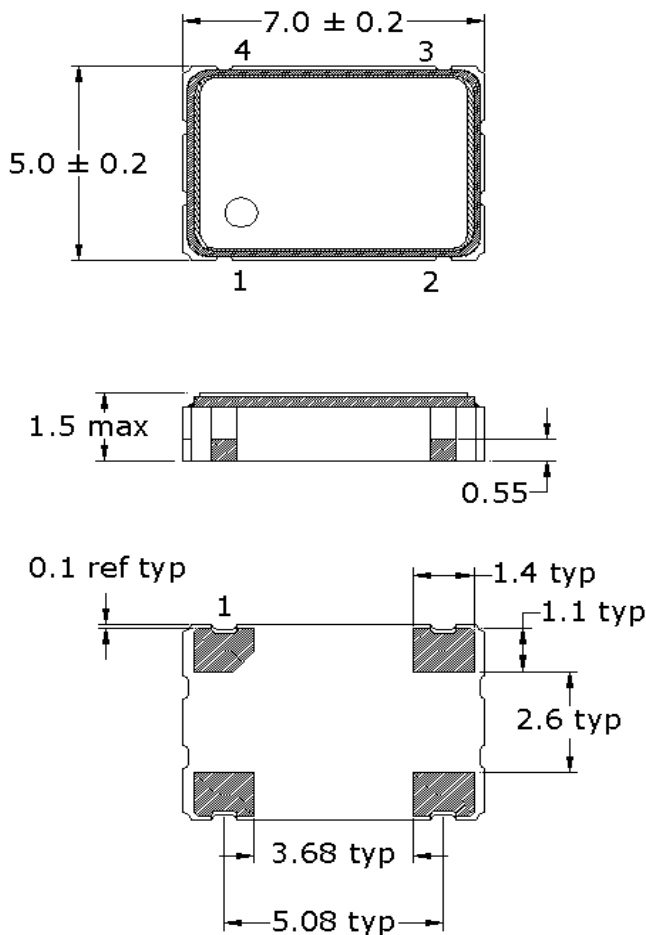
Example: CC065SZ-A2B245-50.0TS

Series Model	Packaging		Operating Temperature	Stability	Symmetry		Frequency (MHz)	Enable/Disable
CC065S	Z	-	A2	B2	45	-	50.0	TS
	Z = Tape/Reel Blank = Tape Only		A2 = -40 ~ +85°C Blank = 0 ~ +70°C	B2 = ±50 ppm Blank = ±100 ppm	45 = 45/55%			TS = Tristate

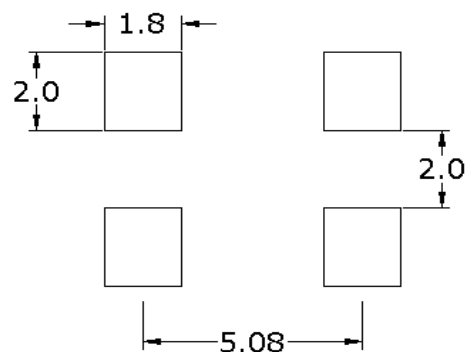
Notes: Specifications with Pad 1 E/D open circuit

¹ Place an appropriate power supply bypass capacitor next to device for correct operation

² Specified by part number

Mechanical Dimensions

Pad Layout

Disclaimer: Recommended layout shown. Adjust layout as needed for individual process requirements.



Dimensions in mm

Contacts (pads): Gold (0.3 to 1.0 μ m) over Nickel (1.27 to 8.89 μ m)

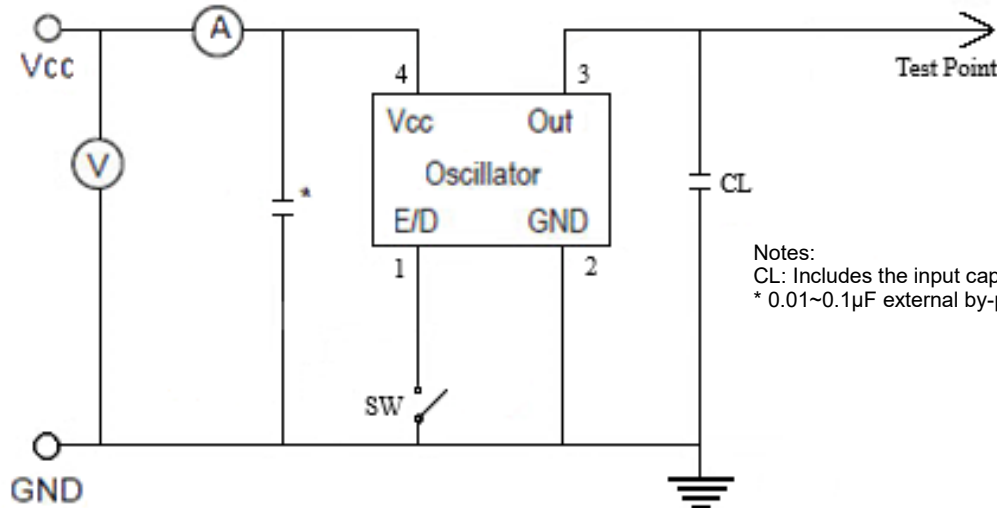
Layout

Pad	Function	Note
1	Output Enable/Disable	The oscillator shall operate when this pad is not connected. The output will be inhibited (high impedance state) when this pad is logic low. Recommend connecting this pad to V_{CC} if the oscillator is to be always on.
2	Ground (GND)	
3	Output	CMOS
4	V_{CC} Supply Voltage	Connect an appropriate power supply bypass capacitor as close as possible

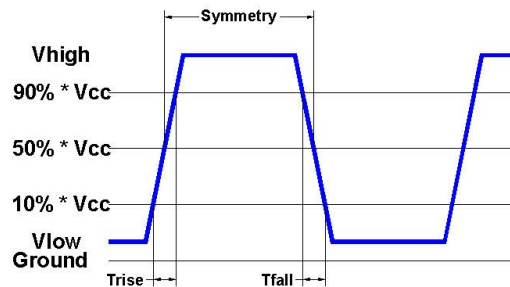
For Optimum Jitter Performance, Cardinal recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Electrical Test / Load Circuit



Notes:
CL: Includes the input capacitance of oscilloscope
* 0.01~0.1 μ F external by-pass filter is recommended



Environmental / ESD Ratings

Reliability: Environmental

ESD Rating

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Solderability	IPC J-STD-002
Thermal Cycle	MIL-STD-883 Method 1010, Condition B

Model	Min. Voltage	Condition
Human Body Model	2000V	JESD22-A114
Machine Model	200V	JESD22-A115

Thermal Characteristics:

The maximum die or junction temperature is 150°C

Absolute Maximum Ratings

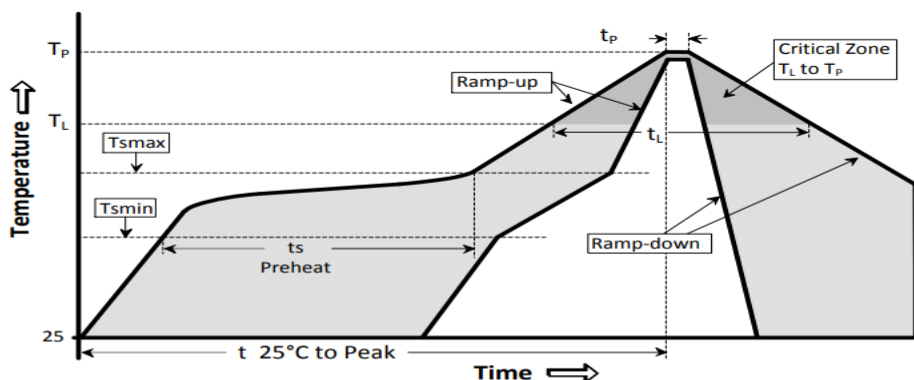
Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +7.0V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V

Cardinal Components Inc. certifies this device is in accordance with the RoHS and REACH directives.

Cardinal Components. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.16 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D
Second Level Interconnect code: e4

Reflow Cycle

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"

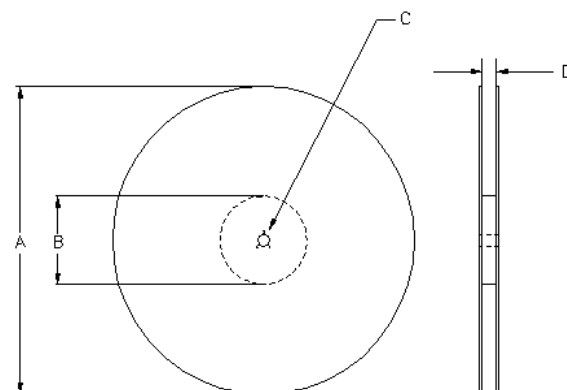
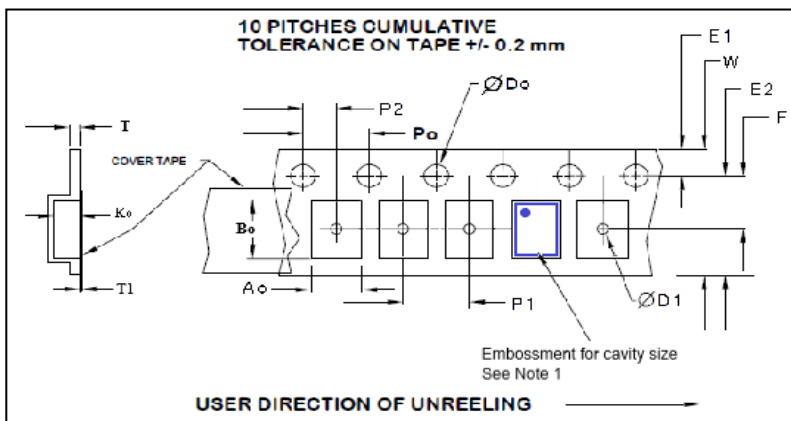


The part may be reflowed 2 times without degradation (typical for lead free processing).

Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(T _{smax} to T _p)	3°C / second max	°C / s
Ramp down Rate	T _{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	T _{to-peak}	8 minutes max	min
Preheat			
Temperature min	T _{smin}	150	°C
Temperature max	T _{smax}	200	°C
Time T _{smin} to T _{smax}	t _s	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T _L	217	°C
Time above liquidus	t _L	60 – 150	sec
Peak temperature			
Peak Temperature	T _p	260	°C
Time within 5°C of peak temperature	t _p	20 – 40	sec

Tape and Reel

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 16mm tape, 8mm pitch.



Tape Variable Dimensions Table 2

Tape Size	E2 typ	F	P1	W max	Ao	Bo	Ko
16mm	14.25	7.5 ±0.05	8.0 ±0.1	16.3	5.56±0.1	7.85±0.1	2.0±0.1

Dimensions in mm Drawing Not to scale

Note 1: Embossed cavity to conform to EIA-481-B

Tape Constant Dimensions Table 1

Tape Size	Do	D1 min	E1	Po	P2	T max	T1 max
16mm	1.5 +0.1 -0.0	1.5	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.3	0.1

Reel Dimensions (may vary) Table 3

	A		B		C	D
Reel Size	Inches	mm	Inches	mm	mm	mm
7	7.0	177.8	2.50	63.5	13.0	Tape size +0.4
10	10.0	254.0	4.00	101.6	+0.5 -0.2	+2.0 -0.0
13	13.0	330.2	3.75	95.3		

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