CARDINAL COMPONENTS

CPP_1 Series
CMOS Clock Oscillator

20.8 x 13.1 x 5.08mm
Metal DIP Package

Features

- CMOS Output (will interface with TTL devices)
- Enable/Disable Function (optional Standby function)
- 3.3V or 5.0V nominal Supply Voltage
- Full DIP14 Package
- Factory programmed

Applications

Driving A/Ds, D/As, FPGAs
Digital Video
Ethernet, GbE
Medical
Storage Area Networking
COTS
Broad Band Access
SONET/ SDH/ DWDM
Test & Measurement

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range	1	-	133	MHz	(3.3V : 1-100MHz)
Frequency Stability [2]	±25	-	±100	ppm	Includes supply voltage change, load change, aging for 1 year at 25°C ± 2°C, shock, vibration and temperatures.
Operating Temperature Range options [2]	0 -20 -40	- - -	+70 +70 +85	°C	
Supply Voltage [1, 2] V_{DD}	2.97	-	5.5	V	See Part Number options on page 2
Supply Current I_{DD} (No Load)	-	-	45 25	mA	V_{DD} = 5.0V V_{DD} = 3.3V
Output Type	CMOS				Cload = 50pF max, V_{DD} = 4.5~5.5V, ≤ 66MHz Cload = 25pF max, V_{DD} = 4.5~5.5V, > 66MHz Cload = 30pF max, V_{DD} = 2.97~3.63V, ≤ 40MHz Cload = 15pF max, V_{DD} = 2.97~3.63V, > 40MHz
	TTL				Cload = 50pF max; V_{DD} = 4.5~5.5V, ≤ 40MHz
Duty Cycle	-	-	-	%	See Page 2
Output V_{OH} (TTL Level)	2.4	-	-	V	V_{DD} = 4.5~5.5V
(CMOS Level)	V_{DD} - 0.4			V	All voltages
Output V_{OL}	-	-	0.4	V	See Load Circuit and waveform page
Output T_{RISE} and T_{FALL}	-	-	-	ns	See page 2
Startup Time	-	-	2	ms	Time for output to reach specified frequency
$V_{DISABLE}$	-	-	0.8 0.2V_{DD}	V	V_{DD} = 4.5~5.5V V_{DD} = 2.97~3.63V
V_{ENABLE}	2.0 0.7V_{DD}	-			V_{DD} = 4.5~5.5V V_{DD} = 2.97~3.63V
Enable Time	-	-	2	ms	
Disable Time - Pin 1 low to Output Hi-Z	-	T/2	T+10	ns	T = Frequency Period
Disable Current	- -	- 0.4	- -	mA	Enable/Disable: Pad 1 low, output disabled; See above Supply Current Standby option: Pad 1 low, output disabled, oscillator shutdown
RMS Period Jitter	-	40 30	50 40	ps	≤ 33MHz > 33MHz
Period Jitter, Pk-Pk		100 75	250 175	ps	>1,000,000 samples ≤ 33MHz > 33MHz
Storage Temperature Range	-55	-	+125	°C	

Notes: Specifications with Pad 1 E/D open circuit
[1] Place an appropriate power supply bypass capacitor next to device for correct operation
[2] Specified by part number

Duty Cycle

Parameter	Min	Typ	Max	Unit	
TTL @1.4V level; V_{DD} = 4.5~5.5V	45 45 40 40		55 55 60 60	%	Fo ≤ 50 MHz, C_L ≤ 50pF 50 MHz < Fo ≤ 66MHz; C_L ≤ 15pF 66 MHz < Fo ≤ 125MHz, C_L ≤ 25pF 125 MHz < Fo ≤ 133MHz, C_L ≤ 15pF

Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V_{DD} level; V_{DD} = 4.5~5.5V	45 40 40		55 60 60	%	Fo ≤ 66 MHz, C_L ≤ 25pF 66 MHz < Fo ≤ 125MHz; C_L ≤ 25pF 125 MHz < Fo ≤ 133MHz, C_L ≤ 15pF

Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V_{DD} level; V_{DD} = 2.97~3.63V	45 40		55 60	%	Fo ≤ 40 MHz, C_L ≤ 30pF 40 MHz < Fo ≤ 100MHz; C_L ≤ 15pF

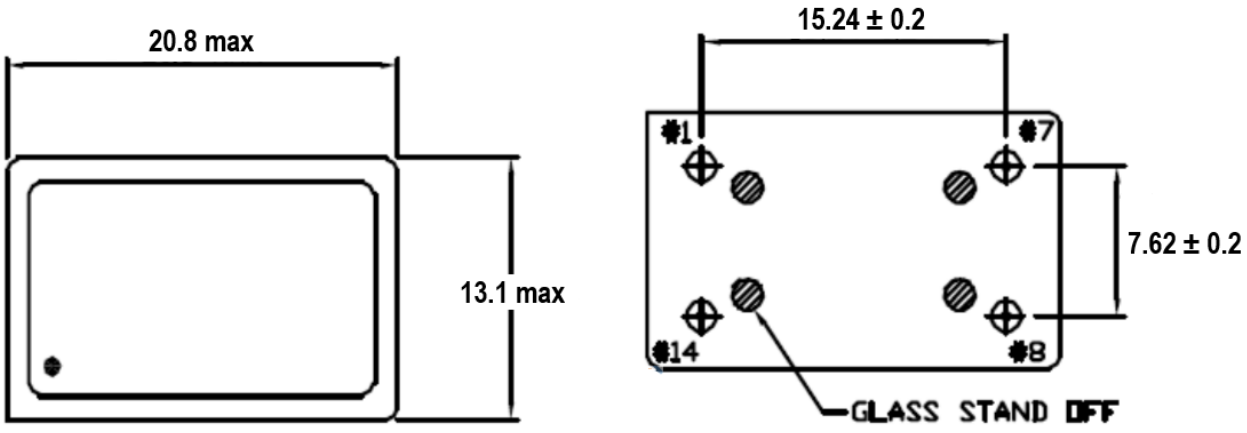
Rise/Fall Time

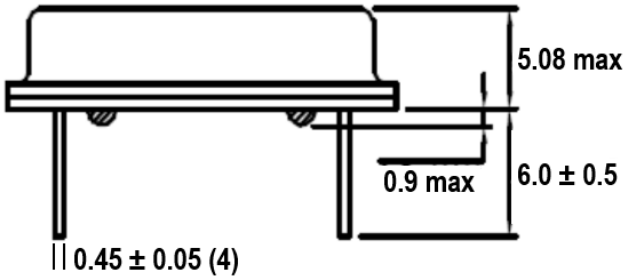
Parameter	Min	Typ	Max	Unit	
Rise/Fall Time			1.8 1.2 0.9 3.4 4.0 2.4	ns	0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=50pF 0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=25pF 0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=15pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 4.5~5.5V, C_L=50pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 2.97~3.63V, C_L=30pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 2.97~3.63V, C_L=15pF

Part Number Example: CPPC1LT-A7BP-50.0TS

Series Model	Logic	Package Size	Supply Voltage V_{CC}	Packaging	Operating Temperature Range	Frequency Stability (ppm)	Frequency (MHz)	Enable/Disable
CPP	**C**	**1**	**L**	**T**	**A7**	**BP**	**50.0**	**TS**
	C=CMOS T = TTL	**1 = Full DIP**	**L = 3.3V** Blank= 5.0V	Blank = Bulk **T = Tube**	Blank = 0 to +70°C A5 = -20 to +70°C **A7 = -40 to +85°C**	BR = ±25 **BP = ±50** B6 = ±100	5V: 1 - 133 3.3V: 1 - 100	**TS = Tristate** PD = Powerdown

Mechanical Dimensions (mm)





Pin #	Function
1	Control
7	GND
8	Output
14	V_{DD}

Pin 1	Output
Open	Active
Logic '1'	Active
Logic '0'/Ground	Tri-state

Termination coating: SnAgCu (SAC305): 2 ~ 7µm

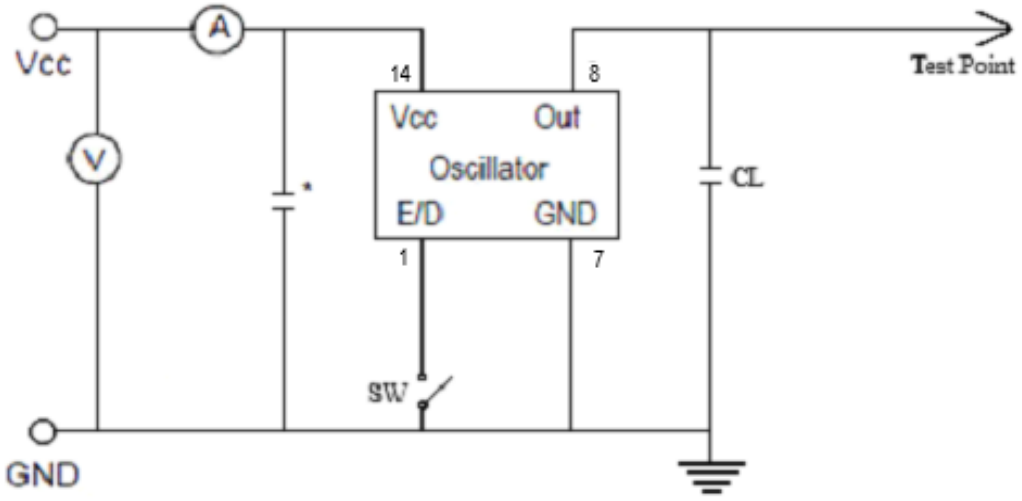
Cardinal Components Inc. certifies this device is in accordance with the RoHS and REACH directives.

Cardinal Components guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 3.5 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D
Second Level Interconnect code: e1

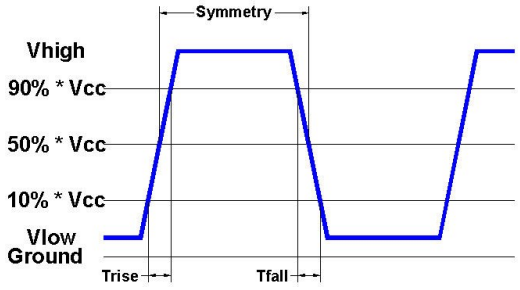
For Optimum Jitter Performance, Cardinal recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Electrical Test / Load Circuit



Notes:
CL: 15pF Includes the input capacitance of oscilloscope
* 0.01~0.1µF external by-pass filter



Environmental / ESD Ratings

Reliability: Environmental

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Solderability	IPC J-STD-002
Thermal Cycle	MIL-STD-883 Method 1010, Condition B

Thermal Characteristics:
The maximum die or junction temperature is 100°C

ESD Rating

Model	Min. Voltage	Condition
Human Body Model	2000V	MIL-STD-883 3015.7
Machine Model	200V	EIAJ ED-4701/304

Absolute Maximum Ratings

Parameter	Unit
V_{CC} Supply Voltage	-0.5V to +7.0V
Vi Input Voltage	-0.5V to V_{CC} + 0.5V
Vo Output Voltage	-0.5V to V_{CC} + 0.5V

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