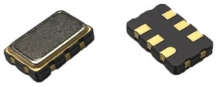
CARDINAL COMPONENTS

CJVAC5L SERIES CMOS VCXO



CJVAC5
5.0 x 3.2 x 1.25 mm
LCC Ceramic Package

Features

- Quartz crystal controlled Precision Square Wave Oscillator
- CMOS Output
- Voltage Control function
- Enable/Disable Function on pad 2
- 3.3V nominal Supply Voltage
- 10MHz - 250MHz frequency range

Applications

Driving A/Ds, D/As, FPGAs
Fibre Channel
Ethernet, GbE, SynchE
Medical
Storage Area Networking
COTS
Telecom
PON

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range [2]	10	-	250	MHz	
Frequency pullability **APR** [2]	±50	-	-	ppm	Absolute pull range, includes effect of temperature stability
Operating Temperature Range [2]	-20 -40	-	+70 +85	°C	
Supply Voltage [1, 2] V_{CC}	2.97	3.3	3.63	V	TVcc ramp = 100µs min
Supply Current I_{CC}	-	-	40 50	mA	10 MHz ~ < 160 MHz 160 MHz ~ ≤ 250 MHz
Output Waveform	CMOS				
Output Voltage High V_{OH}	2.97	-	-	V	
Output Voltage Low V_{OL}	-	-	0.33	V	
Output T_{RISE} and T_{FALL}	-	-	2.0	ns	Vth is 10% and 90% of Vcc
Startup Time	-	-	2	ms	Time for output to reach specified frequency
Duty Cycle	45	-	55	%	Referenced to 50% of amplitude or crossing point
$V_{DISABLE}$	-	-	0.3*Vcc	Volts	Referenced to Ground
V_{ENABLE}	0.7*Vcc	-	-		
Enable Time	-	-	200	ns	< 50MHz
	-	-	100	ns	≥ 50MHz
Disable Time	-	-	50	ns	Time for output to reach a high Z state
Control Voltage	0	1.65	3.3		Vc Input Impedance = 1MΩ min
Modulation Bandwidth	10	-	-	kHz	
Linearity	-	-	10	%	
Aging	-	-	±3.0	ppm	per year
Storage Temperature Range	-55	-	+125	°C	

Notes: Specifications with Pad 2 E/D open circuit
[1] Place an appropriate power supply bypass capacitor next to device for correct operation
[2] Defined by part number

Typical Phase Noise/Jitter

Phase Noise	10 Hz 100 Hz 1 kHz 1 MHz 20 MHz	-66 -96 -112 -136 -154	dBc/Hz	**Precision Developed Frequencies: 25, 50, 100, 106.25, 120, 150, 156.25** 25°C ± 2°C at 2.5V / 156.250 MHz
Jitter		0.6	ps rms	12 kHz to 20 MHz from the output frequency @ 156.25Mhz
Phase Noise	10 Hz 100 Hz 1 kHz 1 MHz 20 MHz	-51 -88 -108 -135 -151	dBc/Hz	**All Other Frequencies** 25°C ± 2°C at 2.5V / 133 MHz
Jitter		2.4	ps rms	12 kHz to 20 MHz from the output frequency @133MHz

Part Number (Example: CJVAC5LZ-A7BP-50.0TS)

Series Model	Logic	Package size	Supply Voltage	Packaging	Operating Temperature Range	Pullability (APR)	Frequency MHz	Enable/ Disable
CJVA	**C**	**5**	**L**	**Z**	**A7**	**BP**	**50.0**	**TS**
	C = CMOS	**5 = 5 x 3.2mm**	**L = 3.3V**	Blank = Tape Only **Z = Tape/Reel**	A5 = -20 to +70°C **A7 = -40 to +85°C**	**BP = ±50 ppm min**	10 - 250 MHz	**TS=Tristate**

Cardinal Components Inc. certifies this device is in accordance with the RoHS and REACH directives.

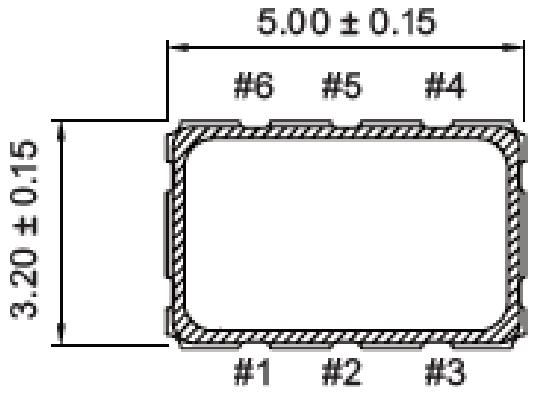
Cardinal Components Inc. guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.09 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D
Second Level Interconnect code: e4

For Optimum Jitter Performance, Cardinal recommends:

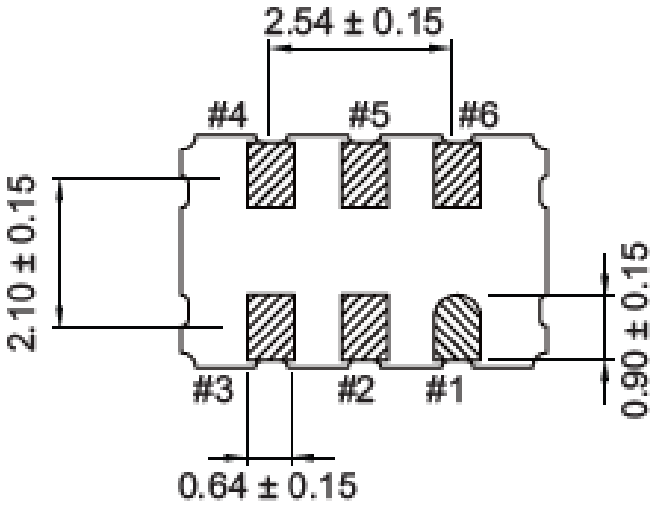
- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Mechanical Dimensions (mm)

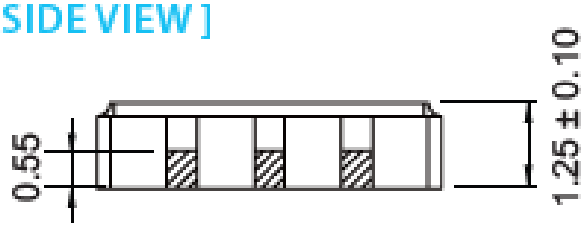
[TOP VIEW]



[BOTTOM VIEW]

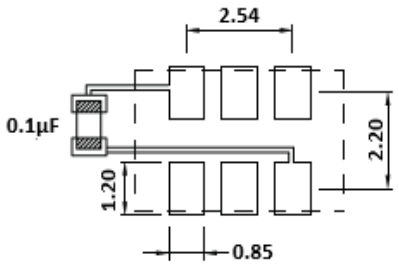


[SIDE VIEW]



Pin#	Function
1	Vcon
2	Tri-State
3	GND
4	Output
5	NC
6	VDD

Contacts (pads): Gold (0.3 to 1.0 µm) over Nickel (1.27 to 8.89 µm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

Pad Layout mm shown

Disclaimer: Recommended layout shown. Adjust layout as needed for individual process requirements.

Enable/Disable	
Pin2	**Output**
Open	Active
Logic '1'	Active
Ground/Logic '0'	Tri-state

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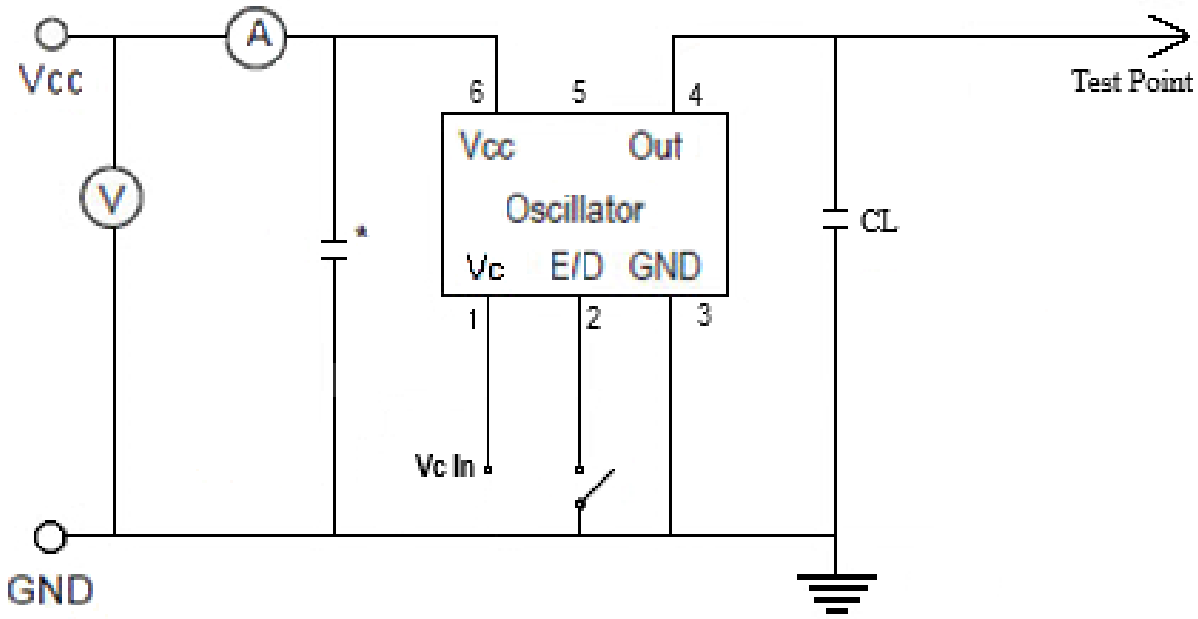
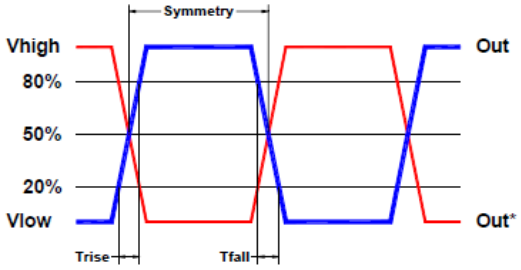
Electrical Test /Load Circuit



Test Waveform



Showing Out Measurement only

Environmental / ESD Ratings

Reliability: Environmental

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Solderability	IPC J-STD-002
Thermal Cycle	MIL-STD-883 Method 1010, Condition B

ESD Rating

Model	Min. Voltage	Condition
Human Body Model	2000V	JESD22-A114
Charged Device Model	1000V	JESD22-C101
Machine Model	120V	JESD22-A115

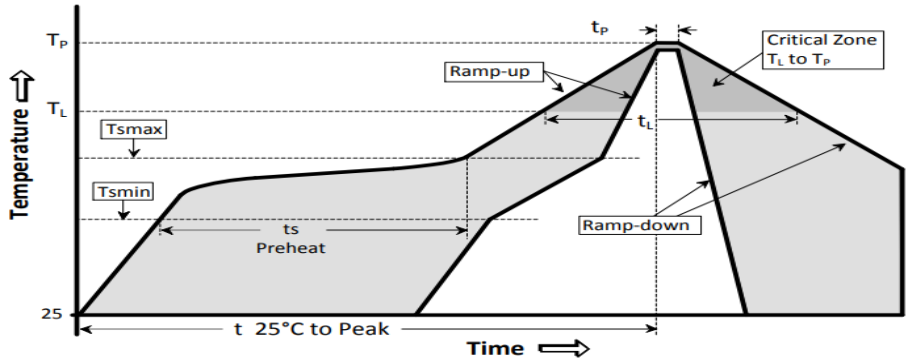
Thermal Characteristics:
The maximum die or junction temperature is 125°C

Absolute Maximum Ratings

Parameter	Unit
V_{CC} Supply Voltage	-0.5V to +4.2V
Vi Input Voltage	-0.5V to V_{CC} + 0.5V
Vo Output Voltage	-0.5V to V_{CC} + 0.5V

Reflow Cycle

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"

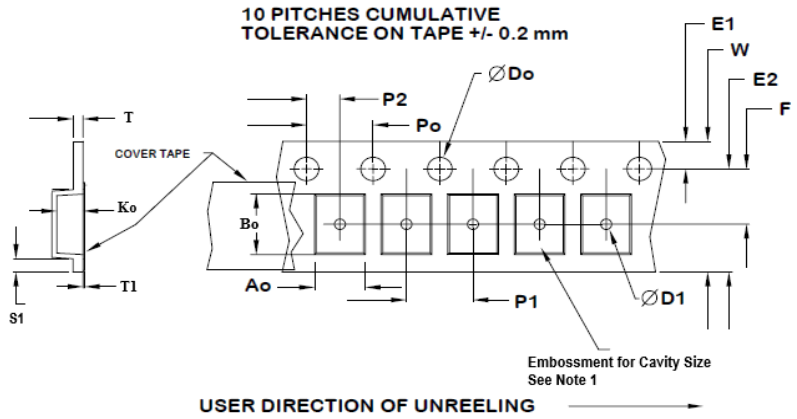


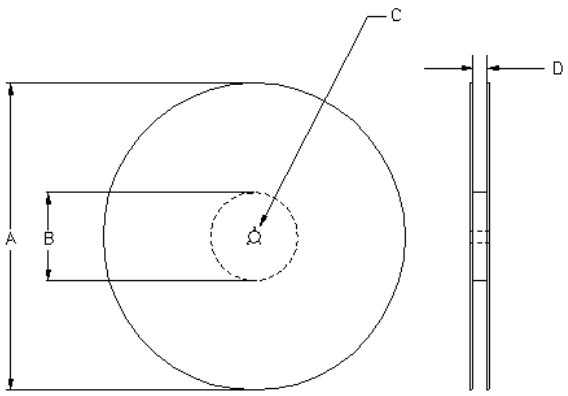
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to T_P)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	min
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 – 40	sec

The part may be reflowed 2 times without degradation (typical for lead free processing).

Tape and Reel

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 12mm tape, 8mm pitch.





Tape Variable Dimensions Table 2							
Tape Size	E2 typ	F	P1	W max	Ao	Bo	Ko
12mm	10.25	5.5 ±0.05	8.0 ±0.1	12.2	3.6±0.1	5.4±0.1	1.4±0.1

Dimensions in mm Drawing Not to scale

Note 1: Embossed cavity to conform to EIA– 481-B

Tape Constant Dimensions Table 1								
Tape Size	Do	D1	E1	Po	P2	S1 min	T max	T1 max
12mm	1.5 +0.1 -0.0	1.5	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.3	0.1

Reel Dimensions (may vary) Table 3						
	A		B		C	D
Reel Size	Inches	mm	Inches	mm	mm	mm
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 +2.0 -0.0
10	10.0	254.0	4.00	101.6		
13	13.0	330.2	3.75	95.3		

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