

CTXXPC3
3.2 x 2.5 x 1.6 mm
Leadless Ceramic Package

Features

- Quartz crystal controlled PLL Based TCXO
- CMOS Output
- Enable/Disable Function on pad 2
- 2.5V and 3.3V Supply Voltages

Applications

Driving A/Ds, D/As, FPGAs
Fibre Channel
Ethernet, GbE, SynchE
SONET
Storage Area Networking
Broadband
Telecom
Smart Grid

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range	10		250	MHz	
Frequency Stability	±2.0	-	±2.5	ppm	Specified by part number; $(f_{\max} - f_{\min}) / 2$
Operating Temperature Range	-40	-	+85	°C	See Part Number guide for options
Storage Temperature Range	-55		+125	°C	
Supply Voltage ¹ V _{DD}	2.375 2.97	2.5 3.3	2.625 3.63	V	TV _{CC} ramp = 100µs min
Supply Current I _{DD}	-	20	40	mA	CL = 15 pF
Disable Current	-	16	-	mA	Pin 2 low
Output Waveform	CMOS				CL = 15 pF
Output High Voltage (V _{OH})	0.9*V _{CC}	-	-	V	
Output Low Voltage (V _{OL})	-	-	0.1*V _{CC}	V	
Output T _{RISE} and T _{FALL}			0.6	ns	V _{th} is 10% and 90% of V _{DD}
Startup Time	-	-	10	ms	Time for output to reach specified frequency
Duty Cycle	45	-	55	%	At 50% V _{CC} level
Enable/Disable Pullup	-	900	-	kΩ	Pin 2 to V _{DD}
V _{DISABLE}	-	-	0.3*V _{CC}	V	Referenced to Ground
V _{ENABLE}	0.7*V _{CC}	-	-		
Phase Noise	1 kHz 10 kHz 100 kHz 1 MHz 10 MHz 20 MHz	-	-111 -118 -119 -134 -155 -156	-	dBc/Hz 25°C ± 2°C, 3.3V, 155.52MHz
Phase Jitter	-	0.9	-	ps rms	12 kHz to 20 MHz at 155.52 MHz

Part Number

Example: CTXXPC3LZLD-100.0

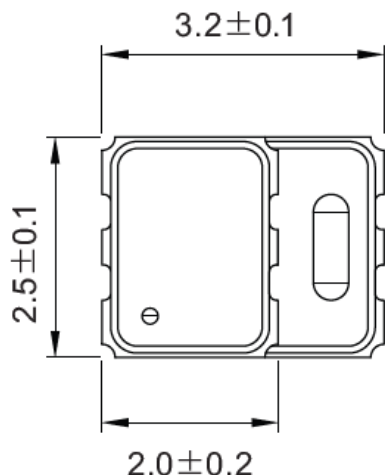
Series Model	Output	Package Size	Supply Voltage	Packaging	Operating Temperature Range	Frequency Stability	Frequency (MHz)
CTXXP	C	3	L	Z	L	D	100.0
	C = CMOS	3 = 3.2x2.5mm	S = 2.5V L = 3.3V	Blank = Tape only Z = Tape/Reel	C = -20 to +70°C H = -30 to +75°C D = -30 to +85°C L = -40 to +85°C	C = ±2.0 ppm D = ±2.5 ppm	

Notes: Specifications with Pad 1 E/D open circuit

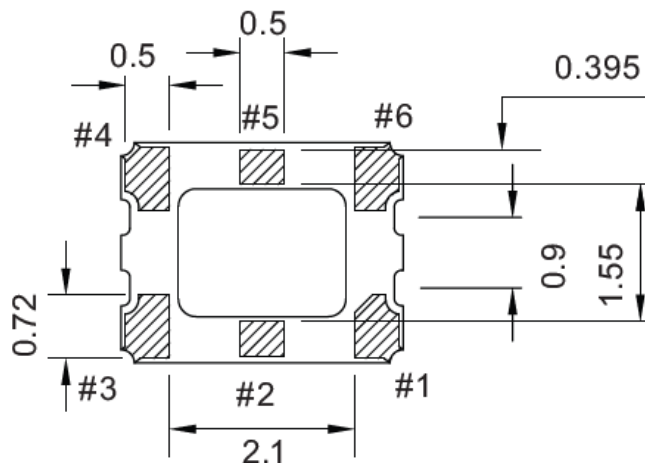
¹ Place an appropriate power supply bypass capacitor next to device for correct operation

Mechanical Dimensions (mm)

[TOP VIEW]



[BOTTOM VIEW]



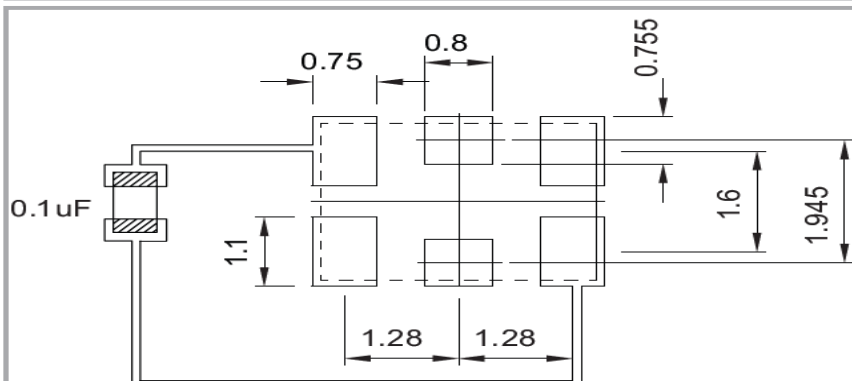
[SIDE VIEW]



Type	CMOS
Pad	Function
1	No Connection
2	Tri-State
3	GND
4	Output
5	No Connection
6	VDD

Enable/Disable	
Pin 2	Output
Open	Active
Logic '1'	Active
Ground	Tri-state

Contacts (pads): Gold (0.3 to 1.0 μm) over Nickel (1.27 to 8.89 μm)



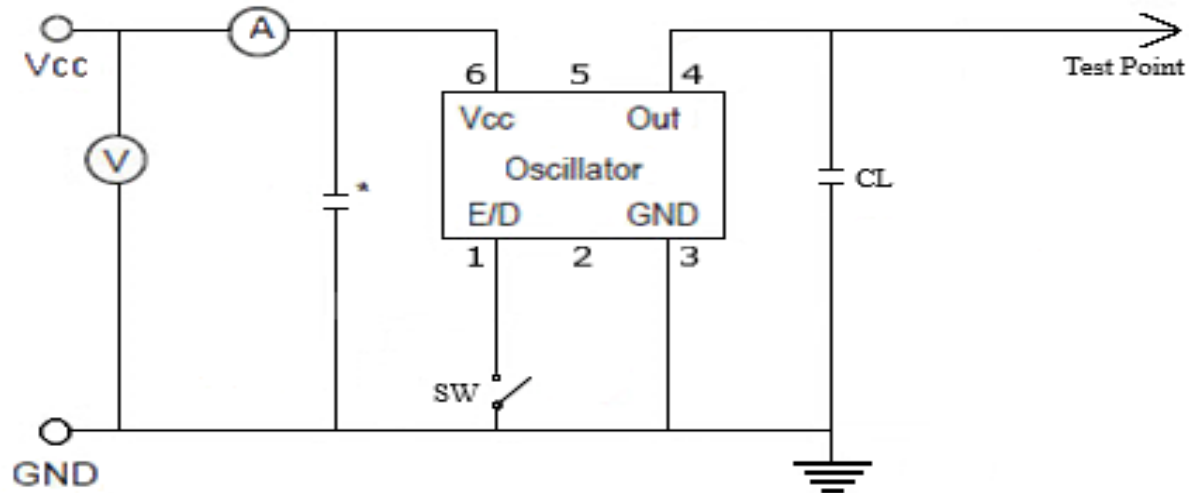
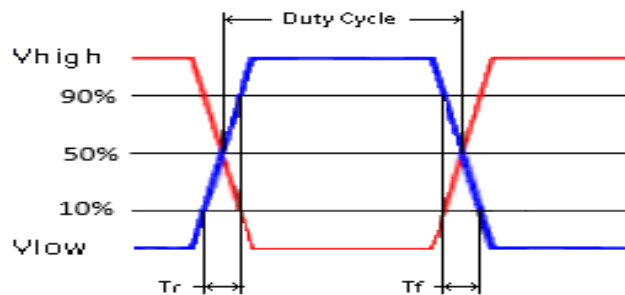
To ensure optimal oscillator performance, place a by-pass capacitor of 0.1 μF as close to the part as possible between Vdd and GND pads.

Pad Layout mm shown

Disclaimer: Recommended layout shown. Adjust layout as needed for individual process requirements.

For Optimum Jitter Performance, Cardinal recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Electrical Test /Load Circuit

Test Waveform

Environmental / ESD
Reliability: Environmental Test

Parameter	Reference Standard	Test Condition
Vibration	MIL-STD-883 2007 Condition A	10-2000Hz, 1.52mm, 20g, each axis for 4hrs
Thermal Shock	MIL-STD-883 1010 Condition B	-55°C, 125°C, soak time is 10 mins, with total 200 cycles
Mechanical Shock	MIL-STD-883 2002 Condition B	1500g, half-sine, 0.5ms, each axis for 3 times

Absolute Maximum Ratings

Parameter	Unit
V _{CC} Supply Voltage	-0.5V to +4.2V
V _i Input Voltage	-0.5V to V _{CC} + 0.5V
V _o Output Voltage	-0.5V to V _{CC} + 0.5V
Max Junction Temperature	125°C

ESD Rating

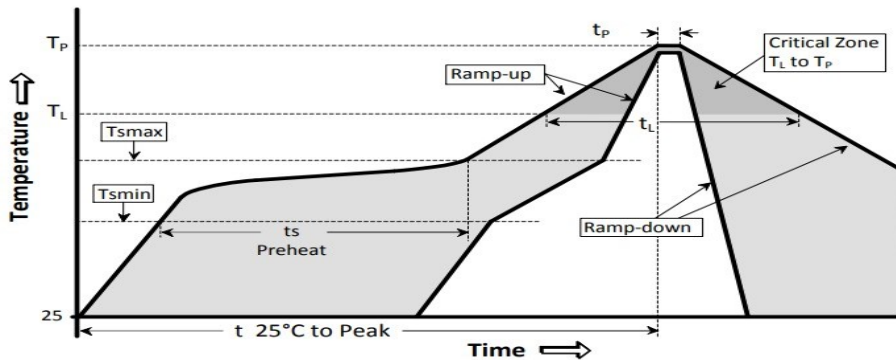
Model	Min. Voltage	Condition
Human Body Model	2000V	JESD22-A114
Charged Device Model	1000V	JESD22-C101
Machine Model	120V	JESD22-A115

Cardinal Components certifies this device is in accordance with the RoHS and REACH directives.

Cardinal Components guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
 Weight of the Device: 0.028 grams
 Moisture Sensitivity Level: 1 As defined in J-STD-020D
 Second Level Interconnect code: e4

Reflow Cycle

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"

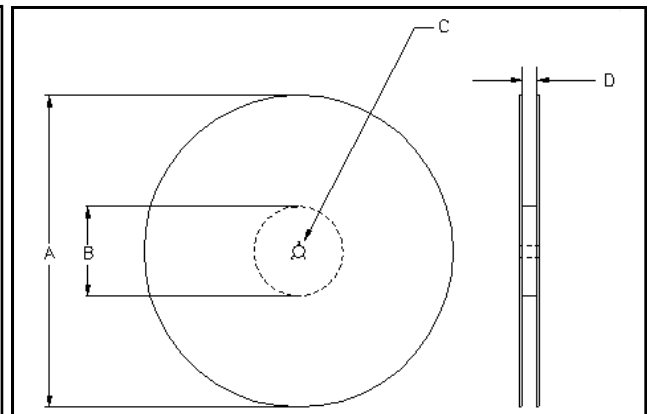
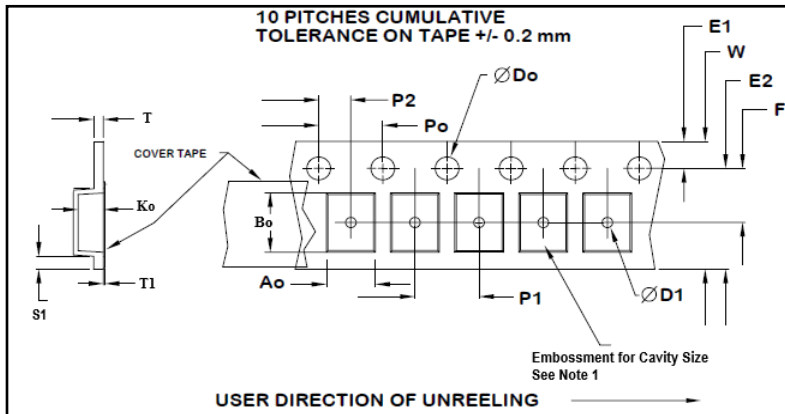


The part may be reflowed 2 times without degradation (typical for lead free processing).

Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	$(T_{smax} \text{ to } T_P)$	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to-peak}$	8 minutes max	min
Preheat			
Temperature min	T_{smin}	150	°C
Temperature max	T_{smax}	200	°C
Time T_{smin} to T_{smax}	t_s	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	T_P	260	°C
Time within 5°C of peak temperature	t_P	20 – 40	sec

Tape and Reel

Tape and Reel available for quantities of 250 to 3000 per reel, cut tape for < 250. 12mm tape, 4mm pitch.



Tape Variable Dimensions Table 2

Tape Size	E2 typ	F	P1	W max	Ao	Bo	Ko
12mm	10.25	5.5 ± 0.05	4.0 ± 0.1	12.2	2.9 ± 0.1	3.6 ± 0.1	1.7 ± 0.1

Dimensions in mm Drawing Not to scale

Note 1: Embossed cavity to conform to EIA-481-B

Tape Constant Dimensions Table 1

Tape Size	Do	D1 typ	E1	Po	P2	S1 min	T max	T1 max
12mm	1.5 +0.1 -0.0	1.5	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.3	0.1

Reel Dimensions (may vary) Table 3

Reel Size	A		B		C	D
	Inches	mm	Inches	mm	mm	mm
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 -0.0

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