Part Number: CRTCP-N05

Real-Time Clock, Calendar with EnerChip™ Battery and 5µAh Integrated Power Management

1. Features

- Power Manager with Charge Control
- Integrated 5µAh Solid State Battery
- Built-in Energy Storage Protection
- Temperature Compensated Charge Control
- Adjustable Switchover Voltage
- Charges EnerChip™ Over a Wide Supply Range
- Low Standby Power
- SMT - Lead-Free Reflow Tolerant
- Thousands of Recharge Cycles
- Low Self-Discharge
- Eco-Friendly, RoHS Compliant – tested
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.0V to 3.3V
- Low backup current: typical 96 HRS
- 2 line bidirectional 1MHz Fast-mode Plus (Fm+) I^2C interface, read D1h, write D0h[2]
- Battery backup and switch-over circuit
- Freely programmable timer and alarm with interrupt capability
- Internal Power-On Reset (POR)
- Open-drain interrupt or clock output pins
- Programmable offset register for frequency adjustment

2. Applications

- Standby Supply
- Wireless sensors and RFID tags
- Localized power Bridging
- Consumer appliances
- Business and industrial systems
- Energy harvesting
- Time keeping application
- Battery powered devices
- Metering
- Telemedicine
- Time stamping
- Smart energy
- Security camera
- Military surveillance
- Data logging

145 Rt. 46 West
Wayne, NJ 07470
Tel: (973)785-1333

E-Mail: sales@cardinalxtal.com
Web: www.cardinalxtal.com

3. General Description

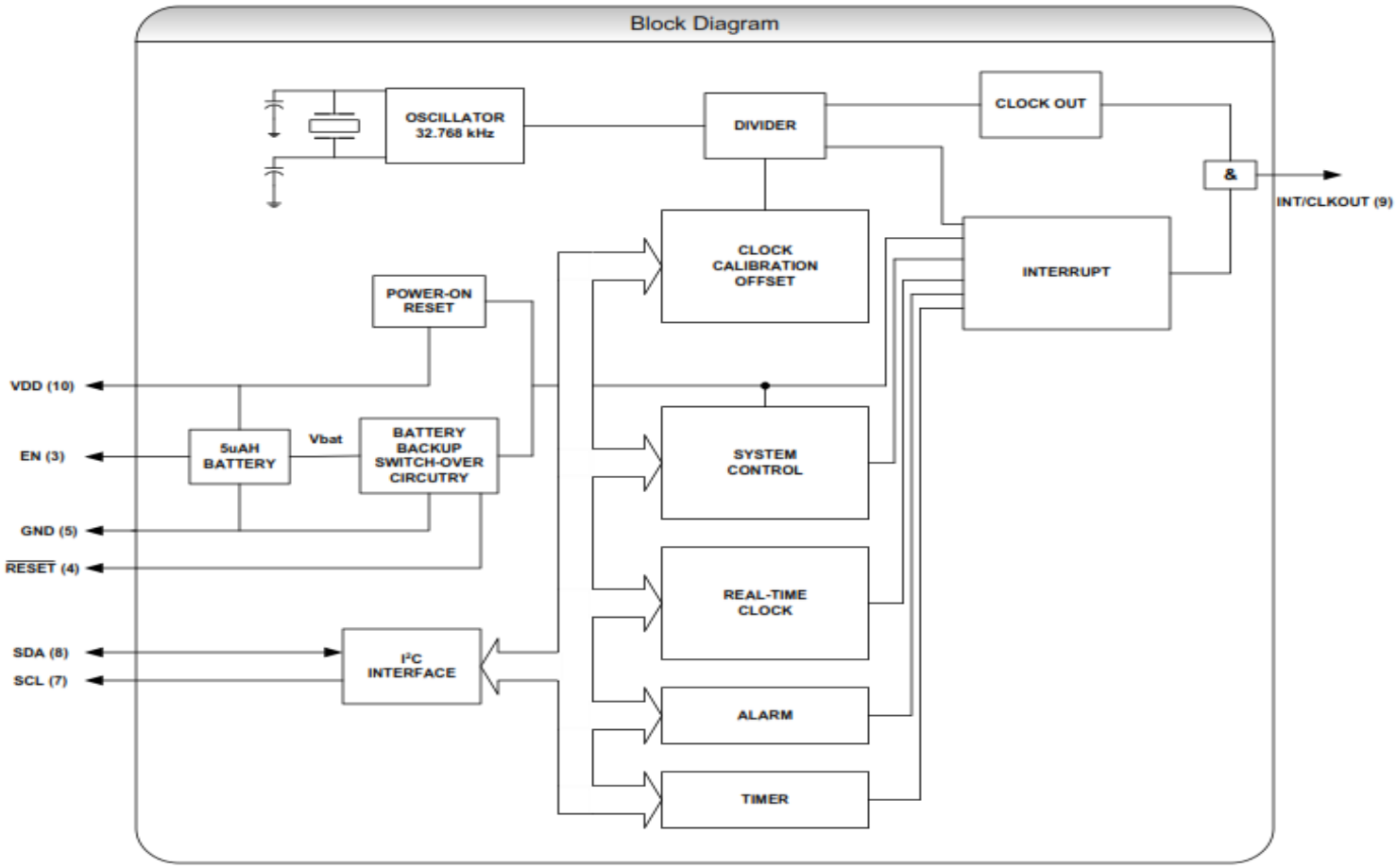
The EnerChip™ CC is the world's first Intelligent Thin Film Energy Storage Device. It is an integrated solution that provides backup energy storage and power management for systems requiring power bridging and/or secondary power.

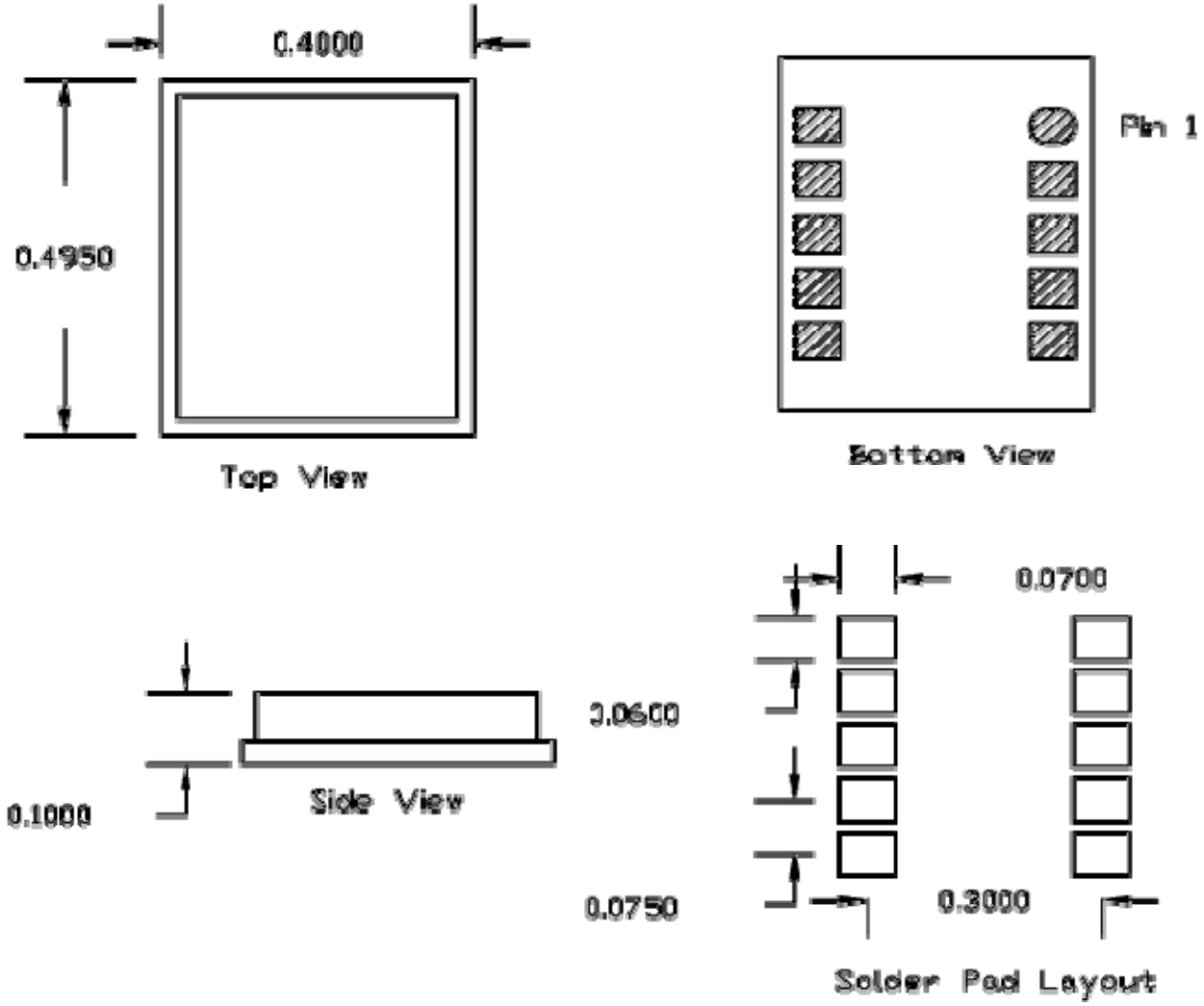
During normal operation, the EnerChip™ CC charges itself with a controlled voltage using an internal charge pump that operates from 2.5V to 3.3V. An ENABLE pin allows for activation and deactivation of the charge pump using an external control line in order to minimize current consumption and take advantage of the fast recharge time of the EnerChip™.

When the primary power supply dips below a user defined threshold voltage, the EnerChip™ CC will signal this event and route the EnerChip™ voltage to V_{OUT}. The EnerChip™ CC also has energy storage protection circuitry to enable thousands of recharge cycles.

The CRTCP-N05 is a Real-Time Clock (RTC) and calendar optimized for low power consumption. Data is transferred serially via an I^2C-bus with a maximum data rate of 1000kbits/s. Alarm and time functions are available with the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine-tuning of the clock. The CRTCP-N05 has a backup battery switch-over circuit, which detects power failures and automatically switches to the battery supply when a power failure occurs.

4. Block Diagram





All dimensions are in inches.

Pin 1	Factory Use Do Not Connect
Pin 2	NC
Pin 3	Enable
Pin 4	/Reset
Pin 5	GND
Pin 6	Factory Use Do Not Connect
Pin 7	SCL
Pin 8	SDA
Pin 9	INT/ F_{OUT}
Pin 10	V_{DD}

5. Functional Description

The CRTCP-N05 contains:

- 20 8-bit registers with an auto-incrementing addresses register
- An on-chip 32.768kHz oscillator with two integrated load capacitors
- A frequency divider, which provides the source clock for the Real-Time Clock (RTC)
- A programmable clock output
- A 1Mbit/s I^2C-bus interface
- An offset register, which allows fine-tuning of the clock

All 20 registers are designed as addressable 8-bit registers although not all bits are implemented.

- The first three registers (memory address 00h, 01h, and 02h) are used as control and status registers.
- The addresses 03h through 09h are used as counters for the clock function (seconds up to years)
- Addresses 0Ah through 0DH define the alarm condition
- Addresses 0Eh defines the offset calibration
- Addresses 0Fh defines the clock-out mode and the addresses 10h and 12h the timer mode
- Addresses 11h and 13h are used for the timers

The registers Seconds, Minutes, Hours, Days, Weekends, Months, and Years are all coded in Binary Coded Decimal (BCD) format. Other registers are either bit-wise or standard binary. When one of the RTC registers is read, the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

The battery switch-over circuit monitors the main power supply and switches automatically to the backup battery when a power failure condition is detected. Accurate timekeeping is maintained even when the main power supply is interrupted.

5.1 Registers Overview

The 20 registers of the XXX are auto-incrementing after each read or write data byte up to register 13h. After register 13h, the auto-incrementing will wrap around to address 00h (see Figure 1, Section 5).

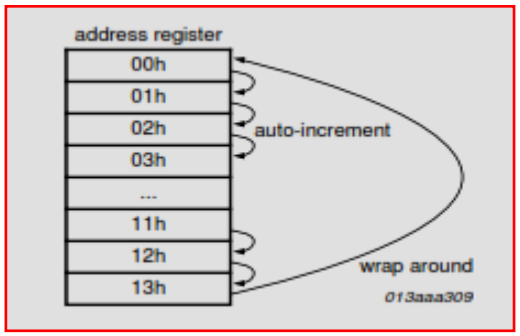


Figure 1, Section 5. Auto Incrementing of the Registers

Table 1, Section 5. Registers Overview 1

Bit positions labeled as "-" are not implemented and will return a 0 when read. Bit "T" must always be written with logic 0.

Address	Register Name	Bit 7	6	5	4	3	2	1	0
Control Register									
00h	Control 1	CAP_SEL	T	STOP	SR	12_24	SIE	AIE	CIE
01h	Control 2	WTAF	CTAF	CTBF	SF	AF	WTAIE	CTAIE	CTBIE
02h	Control 3	PM [2:0]			-	BSF	BLF	BSIE	BLIE
Time and Data Registers									
03h	Seconds	OS	Seconds (0 to 59)						
04h	Minutes	-	Minutes (0 to 59)						
05h	Hours	-	-	AMPM	Hours (1 to 12 in 12 hour mode)				
				Hours (0 to 23 in 24 hour mode)					
06h	Days	-	-	Days (1 to 31)					
07h	Weekdays	-	-	-	-	-	Weekdays (0 to 6)		
08h	Months	-	-		Months (1 to 12)				
09h	Years	Years (0 to 99)							
Alarm Registers									
0Ah	Minutes_Alarm	AE_M	Minute_Alarm (0 to 59)						
0Bh	Hour_Alarm	AE_H	-	AMPM	Hour_Alarm (1 to 12 in 12 hour mode)				
			-	Hour_Alarm (0 to 23 in 24 hour mode)					
0Ch	Day_Alarm	AE_D	-	Day_Alarm (1 to 31)					
0Dh	Weekday_ Alarm	AE_W	-	-	-	-	Weekday_Alarm (0 to 6)		
Offset Register									
0Eh	Offset	MODE	Offset [6:0]						
Clockout and Timer Registers									
0Fh	Tmr_ Clkout_ctrl	TAM	TBM	COF [2:0]	-	-	TAC [1:0]		TBC
10h	Tmr_A_freq_ctrl	-	-	-	-	-	TAQ [2:0]		
11h	Tmr_A_reg	Timer_a_Value [7:0]							
12h	Tmr_B_freq_ctrl	-	TBW [2:0]			-	TBQ [2:0]		
13h	Tmr_B_reg	Timer_B_Value [7:0]							

5.2 Control and Status Registers

5.2.A Register Control 1

Table 2, Section 5. Control 1 - Control and Status Register 1 (address 00h) Bit Description

Bit	Symbol	Value	Description
7	CAP_SEL	0 [2]	7 pF
6	T	0 [1][2]	unused
5	STOP	0 [1]	RTC time circuits running
		1	RTC time circuits frozen; RTC divider chain flip-flops are asynchronously set logic 0; Clockout at 32.768kHz is still available
4	SR	0 [1][3]	No software reset
		1	Initial software reset
3	12_24	0 [1]	24 hour mode is selected
		1	12 hour mode is selected
2	unused		
1	AIE	0 [1]	Alarm interrupt disabled
		1	Alarm interrupt enabled
0	CIE	0 [1]	No correction interrupt generated
		1	Interrupted pulses are generated at every correction cycle (see Section 5.8)

[1] Default value.
[2] Must always be written with logic 0.
[3] For all software reset, 01011000 (58h) must be sent to register Control 1 (see Section 5.3). Bit SR always returns 0 when read.

5.2.B Register Control 2

Table 3, Section 5. Control 2 - Control and Status Register 2 (address 01h) Bit Description

Bit	Symbol	Value	Description
7	WTAF	0 [1]	No watchdog timer A interrupt generated
		1	Flag set when watchdog timer A interrupt generated: flag is read-only and cleared by reading register Control 2
6	CTAF	0 [1]	No countdown timer A interrupt generated
		1	Flag set when countdown timer A interrupt generated; flag must be cleared to clear interrupt
5	CTBF	0 [1]	No countdown timer B interrupt generated
		1	Flag set when countdown timer B interrupt generated; flag must be cleared to clear interrupt
4	SR	0 [1]	No second interrupt generated
		1	Flag set when second interrupt generated; flag must be cleared to clear interrupt
3	AF	0 [1]	No alarm interrupt generated
		1	Flag set when alarm triggered; flag must be cleared to clear interrupt
2	WTAIE	0 [1]	Watchdog timer A interrupt is disabled
		1	Watchdog timer A interrupt is enabled
1	CTAIE	0 [1]	Countdown timer A interrupt is disabled
		1	Countdown timer A interrupt is enabled
0	CTBIE	0 [1]	Countdown timer B interrupt is disabled
		1	Countdown timer B interrupt is enabled

[1] Default value.

5.2.C Register Control 3

Table 4, Section 5. Control 3 - Control and Status Register 3 (address 02h) Bit Description

Bit	Symbol	Value	Description
7 to 5	PM [2:0]	(see Table 6, Sec 5) [1]	Battery switch-over and battery low detection control
4	-	-	unused
3	BSF	0 [2]	No battery switch-over interrupt generated
		1	Flag set when battery switch-over occurs. Flag must be cleared to clear interrupt
2	BLF	0 [2]	Battery status okay
		1	Battery status low; flag is read-only
1	BSIE	0 [2]	No interrupt generated from battery switch-over flag, BSF
		1	Interrupt generated when BSF is set
0	BLIE	0 [2]	No interrupt generated from battery low flag, BLF
		1	Interrupt generated when BLF is set

[1] Default value is 111.
[2] Default value

5.3 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. Software reset command means setting bits 6, 4, and 3 in register Control 1 (00h) logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 2, Section 5.

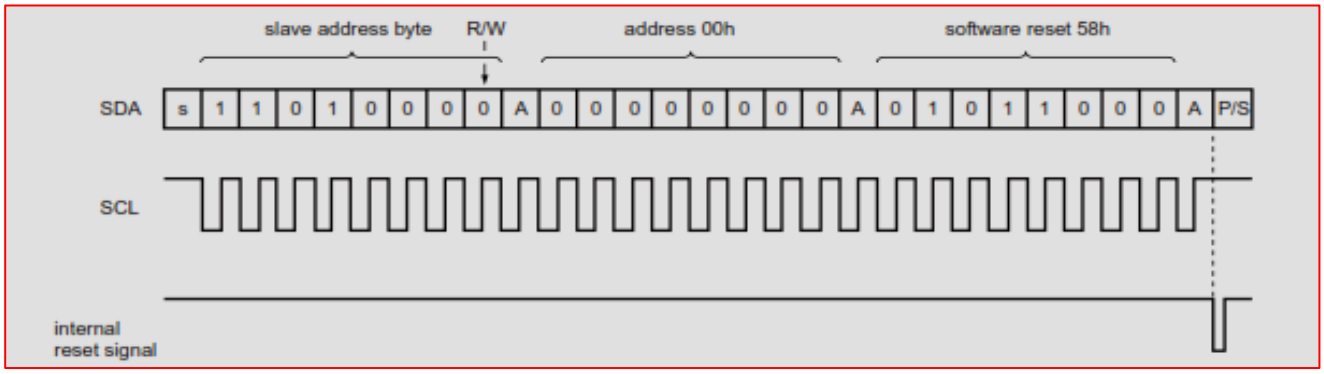


Figure 2, Section 5. Software Reset Command

Table 5, Section 5. Register Reset Values

Bits labeled "X" are undefined at power-on and unchanged by subsequent resets. Bits labeled "-" are not implemented

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00h	Control 1	0	0	0	0	0	0	0	0
01h	Control 2	0	0	0	0	0	0	0	0
02h	Control 3	1	1	1	-	0	0	0	0
03h	Seconds	1	X	X	X	X	X	X	X
04h	Minutes	-	X	X	X	X	X	X	X
05h	Hours	-	-	X	X	X	X	X	X
06h	Days	-	-	X	X	X	X	X	X
07h	Weekdays	-	-	-	-	-	X	X	X
08h	Months	-	-	-	X	X	X	X	X
09h	Years	X	X	X	X	X	X	X	X
0Ah	Minute Alarm	1	X	X	X	X	X	X	X
0Bh	Hour Alarm	1	-	X	X	X	X	X	X
0Ch	Day Alarm	1	-	X	X	X	X	X	X
0Dh	Weekday Alarm	1	-	-	-	-	X	X	X
0Eh	Offset	0	0	0	0	0	0	0	0
0Fh	tmr CLKOUT ctrl	0	0	0	0	0	0	0	0
10h	tmr A freq ctrl	-	-	-	-	-	1	1	1
11h	tmr A reg	X	X	X	X	X	X	X	X
12h	tmr B freq ctrl	-	0	0	0	-	1	1	1
13h	tmr B reg	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768kHz CLKOUT active
- 24 hour mode is selected
- Register Offset is set logic 0
- No alarms set
- Timers disabled
- No interrupts enabled
- Battery switch-over is disabled

5.4 Interrupt Function

Active low interrupt signals are available at pin INT1/CLKOUT. INT1/CLKOUT has both functions of INT1 and CLKOUT combined. INT1 Interrupt output may be sourced from different places:

- Second timer
- Timer A
- Timer B
- Alarm
- Battery switch-over
- Clock offset correction pulse

The control bit TAM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupts generated from the second interrupt timer and timer A are pulsed signals or a permanently active signal. The control bit TBM (register Tmr_CLKOUT_ctrl) is used to configure whether the interrupt generated from timer B is a pulsed signal or a permanently active signal. All the other interrupt sources generate a permanently active interrupt signal, which follows the status of the corresponding flags.

- The flags SF, CTAF, CTBF, AF, and BSF can be cleared by using the interface
- WTAF is read only. Reading of the register Control 2 (01h) automatically resets WTAF (WTAF = 0) and clears the interrupt
- The flag BLF is read only. It is cleared automatically from the battery low detection circuit when the battery is replaced

5.5 Power Management Functions

The power management functions are controlled by the control bits PM [2:0] in register Control 3 (02h).

Table 6, Section 5. Power Management Function Control Bits

PM [2:0]	Function
000	Battery switch-over function is enabled in standard mode;
	Battery low detection function is enabled
001	Battery switch-over function is enabled in direct switching mode;
	Battery low detection function is enabled
010, 011 [1]	battery switch-over function is disabled - only one power supply (V_{DD});
	Battery low detection function is enabled
100	Battery switch-over function is enabled in standard mode;
	Battery low detection function is disabled
101	Battery switch-over function is enabled in direct switching mode;
	Battery low detection function is disabled
110	Not allowed
111 [2][3]	Battery switch-over function is disabled - only one power supply (V_{DD});
	Battery low detection function is disabled

[1] When the battery switch-over function is disabled, the XXX works only with the power supply V_{DD}.
[2] When the battery switch-over function is disabled, the XXX works only with the power supply V_{DD}. V_{BAT} must be put to ground and the battery low detection function is disabled.
[3] Default value.

5.5.A Standby Mode

When the device is first powered up from the battery (V_{BAT}) but without a main supply (V_{DD}), the CRTCP-N05 automatically enters the standby mode. In standby mode, the CRTCP-N05 does not draw any power from the backup battery until the device is powered up from the main power supply V_{DD}. Thereafter, the device switches over to battery backup mode whenever the main power supply V_{DD} is lost.

5.5.B Battery Switch-over Function

The CRTCP-N05 has a backup battery switch-over circuit. It monitors the main power supply V_{DD} and switches automatically to the backup battery when a power failure condition is detected.

One of two operation modes can be selected:

- **Standard mode:** the power failure condition happens when: $V_{DD} < V_{BAT}$ and $V_{DD} < V_{th(sw)bat}$
- **Direct switching mode:** the power failure condition happens when $V_{DD} < V_{BAT}$. Direct switching from V_{DD} to V_{BAT} without requiring V_{DD} to drop below $V_{th(sw)bat}$

$V_{th(sw)bat}$ is the battery switch threshold voltage. Typical value is 2.5V.

Generation of interrupts from the battery switch-over is controlled via the BSIE bit (see Register Control 2). If BSIE is enabled, the INT1 follows the status of bit BLF (see Register Control 3). Clearing BLF immediately clears INT1.

When a power failure condition occurs and the power supply switches to the battery, the following sequence occurs:

1. The battery switch flag BSF (Register Control 3) is set logic 1
2. An interrupt is generated if the control bit BSIE (Register Control 3) is enabled

The battery switch flag BSF can be cleared by using the interface after the power supply has switched to V_{DD}. It must be cleared to clear the interrupt.

The interface is disabled in battery backup operation:

- Interface inputs are not recognized, preventing extraneous data being written to the device
- Interface outputs are high-impedance

5.5.B1 Standard Mode

If $V_{DD} > V_{BAT}$ or $V_{DD} > V_{th(sw)bat}$, the internal power is V_{DD}.
If $V_{DD} < V_{BAT}$ and $V_{DD} < V_{th(sw)bat}$, the internal power supply is V_{BAT}.

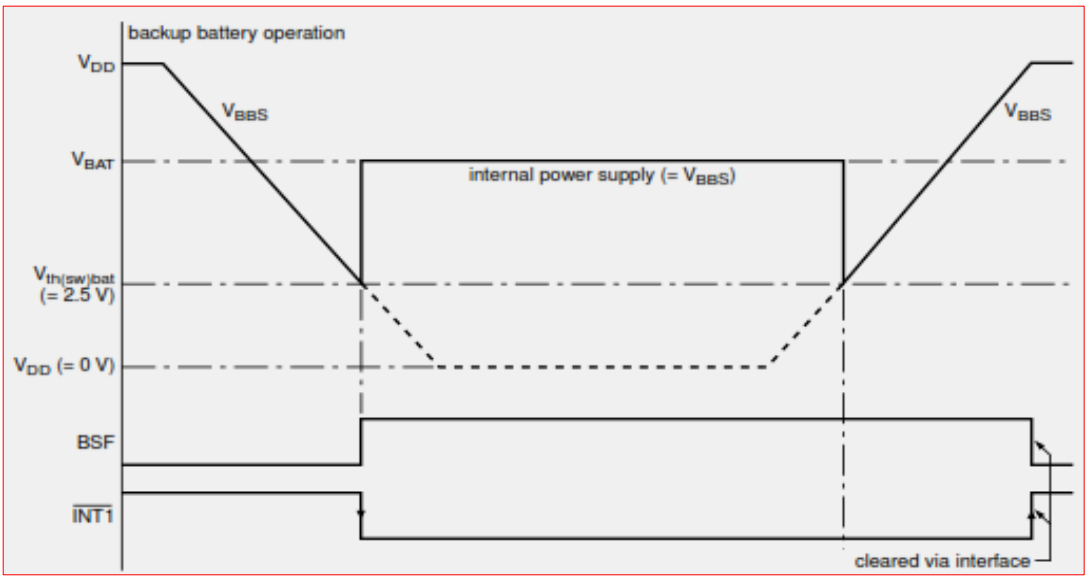


Figure 3, Section 5. Battery switch-over behavior in standard mode and with bit BSIE set logic 1 (enabled)

5.5.B2 Direct Switching Mode

If $V_{DD} > V_{BAT}$ the internal power supply is V_{DD}.

If $V_{DD} < V_{BAT}$ the internal power supply is V_{BAT}.

The direct switching mode is useful in systems where V_{DD} is higher than V_{BAT} at all times (for example, V_{DD} = 5V, V_{BAT} = 3.5V). If the V_{DD} and V_{BAT} values are similar (for example, V_{DD} = 3.3V, $V_{BAT} \geq$ 3.0V), the direct switching mode is not recommended. In direct switching mode, the power consumption is reduced compared to the standard mode because the monitoring of V_{DD} and $V_{th(sw)bat}$ is not performed.

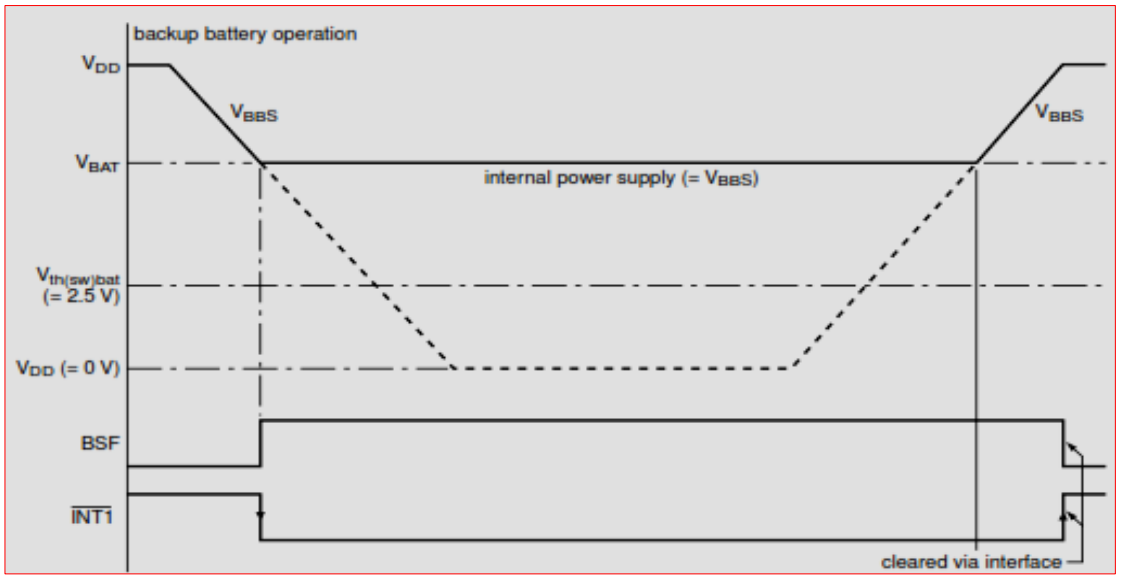


Figure 4, Section 5. Battery switch-over behavior in direct switching mode and with bit BSIE set logic 1 (enabled)

5.5.B3 Battery switch-over disabled, only one power supply (V_{DD})

When the battery switch-over function is disabled:

- The power supply is applied on the V_{DD} pin
- The V_{BAT} pin must be connected to ground
- The battery flag (BSF) is always logic 0

5.6 Time and Date Registers

5.6.A Register Seconds

Table 7, Section 5. Seconds - Seconds and Clock Integrity Status Register (address 03h) Bit Description

Bit	Symbol	Value	Place Value	Description
7	OS	0	-	Clock integrity is guaranteed
		1 [1]	-	Clock integrity is not guaranteed; oscillator has stopped or been interrupted
6 to 4	Seconds	0 to 5	ten's place	Actual seconds coded in BCD format
3 to 0		0 to 9	unit place	

Table 8, Section 5. Seconds Coded in BCD Format

Seconds Value in Decimals	Upper-digit (ten's place)			Digit (unit place)			
	Bit			Bit			
	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

5.6.A1 Oscillator STOP Flag

The OS flag is set whenever the oscillator is stopped (see Figure 5, Section 5). The flag remains set until cleared by using the interface. When the oscillator is not running, then the OS flag cannot be cleared. This method can be used to monitor the oscillator.

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in a range of 200ms to 2s, depending on crystal type, temperature, and supply voltage. At power-on, the OS flag is always set.

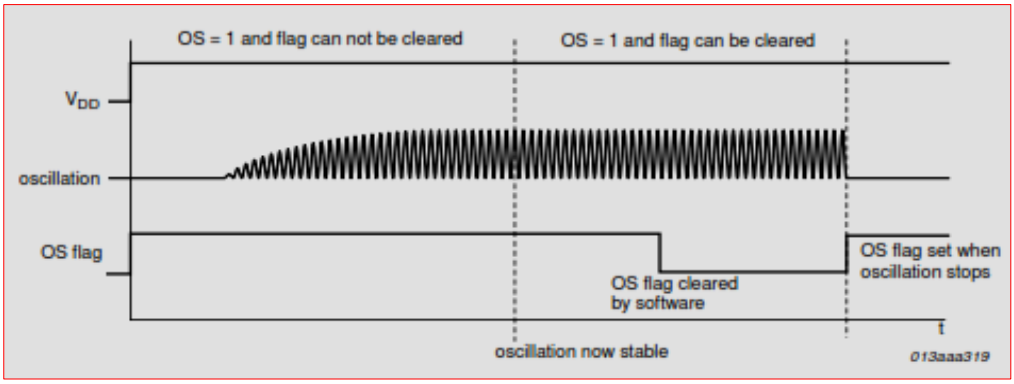


Figure 5, Section 5. OS Flag

5.6.B Register Minutes

Table 9, Section 5. Minutes - Minutes Register (address 04h) Bit Description

Bit	Symbol	Value	Place Value	Description
7	-	-	-	unused
6 to 4	Minutes	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

5.6.C Register Hours

Table 10, Section 5. Hours - Hours Register (address 05h) Bit Description

Bit	Symbol	Value	Place Value	Description
7 to 6	-	-	-	unused
12 Hour Mode [1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 Hour Mode [1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Hour mode is set by bit 12_24 in register Control 1 (see Table 2, Section 5)

5.6.D Register Days

Table 11, Section 5. Days - Days Register (address 06h) Bit Description

Bit	Symbol	Value	Place Value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS [1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] If the year counter contains a value, which is exactly divisible by 4 (including the year 00), the XXX compensates for leap years by adding a 29th day to February.

5.6.E Register Weekdays

Table 12, Section 5. Weekdays - Weekdays Register (address 07h) Bit Description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAY	0 to 6	actual weekday, values see Table 13, Section 5

Table 13, Section 5. Weekday Assignments

Day [1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

5.6.F Register Months

Table 14, Section 5. Months - Months Register (address 08h) Bit Description

Bit	Symbol	Value	Place Value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format; see Table 15, Section 5
3 to 0		0 to 9	unit place	

Table 15, Section 5. Months Assignments in BCD Format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit	Bit			
	4	3	2	1	0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

5.6.G Register Years

Table 16, Section 5. Years - Years Register (09h) Bit Description

Bit	Symbol	Value	Place Value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

5.6.H Data Flow of the Time Function

Figure 6, Section 5. Shows the data flow and data dependencies starting from the 1Hz clock tick.

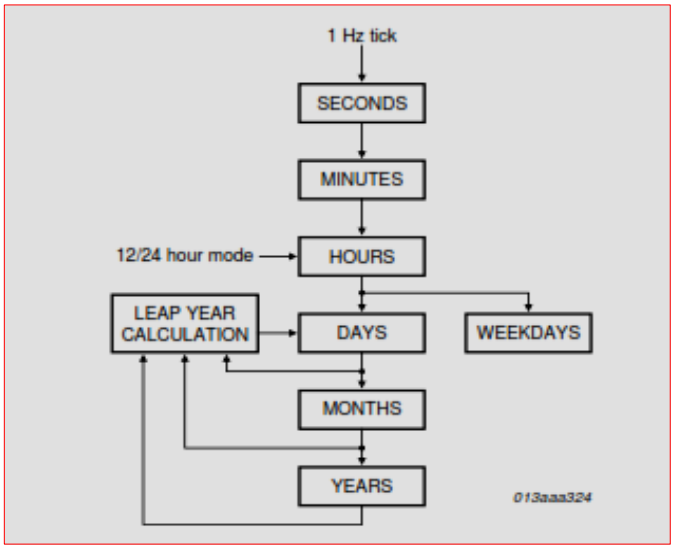


Figure 6, Section 5. Data Flow diagram of the time function

During read/write operations, the time counting circuits (memory locations 03h through 09h) are blocked.

The blocking prevents:

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After the read/write-access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of one request can be stored; therefore, all accesses must be completed within 1 second (see Figure 7, Section 5.)

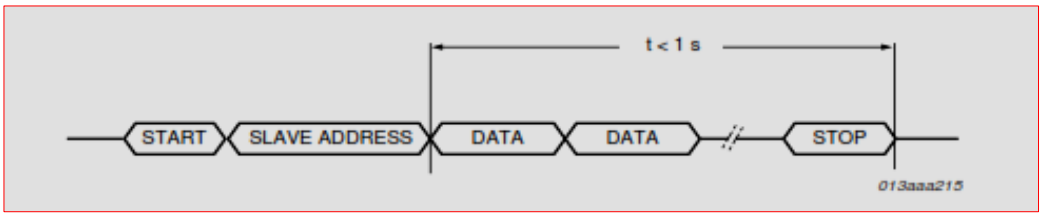


Figure 7, Section 5. Access time for read/write operations

Because of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time will increment between the two accesses. A similar problem exists when reading. A rollover may occur between reads thus giving the minutes from one moment and the hours from the next.

5.7 Alarm Registers

The registers at addresses 0Ah through 0Dh contain the alarm information.

5.7.A Register Minute Alarm

Table 17, Section 5. Minute Alarm - Minute Alarm Register (address 0Ah) Bit Description

Bit	Symbol	Value	Place Value	Description
7	AE_M	0	-	minute alarm is enabled
		1 [1]	-	minute alarm is disabled
6 to 4	Minute_Alarm	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

5.7.B Register Hour Alarm

Table 18 Section 5. Hour Alarm - Hour Alarm Register (address 0Bh) Bit Description

Bit	Symbol	Value	Place Value	Description
7	AE_H	0	-	hour alarm is enabled
		1 [1]	-	hour alarm is disabled
6	-	-	-	unused
12 Hour Mode [2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	Hour_Alarm	0 to 1	ten's place	hour alarm information in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 Hour Mode [2]				
5 to 4	Hours	0 to 2	ten's place	hour alarm information in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.
[2] Hour mode is set by bit 12_24 in register Control 1 (see Table 2, Section 5)

5.7.C Register Day Alarm

Table 19 Section 5. Day Alarm - Day Alarm Register (address 0Ch) Bit Description

Bit	Symbol	Value	Place Value	Description
7	AE_D	0	-	day alarm is enabled
		1 [1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	Day_Alarm	0 to 3	ten's place	day alarm information in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

5.7.D Register Weekday Alarm

Table 20 Section 5. Weekday Alarm - Weekday Alarm Register (address 0Dh) Bit Description

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1 [1]	weekday alarm is disabled
6	-	-	unused
3 to 0	Weekday_Alarm	0 to 6	weekday alarm information

[1] Default value.

5.7.E Alarm Flag

(1) Only when all enabled alarm settings are matching. It is only on increment to a matched case that the alarm flag is set, see Section 5.7.E

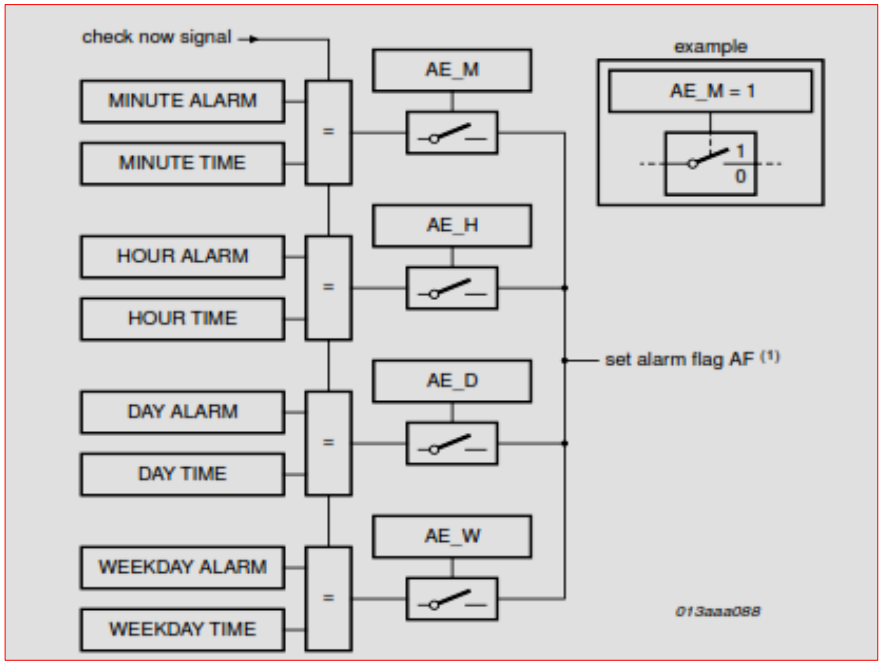


Figure 8, Section 5. Alarm function block diagram

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday value. When all enabled comparisons first match, the alarm flag, AF (Register Control 2), is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (Register Control 1). If bit AIE is enabled, then the INT1 pin follows the condition of bit AF. AF remains set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers, which have their AE_x bit logic 1, are ignored. The generation of interrupts from the alarm function is described in more detailed in Section 3.4.

Table 21and Table 22, Section 3 show an example for clearing bit AF. Clearing the flag is made by a write command, therefore bits 2, 1, and 0 must be re-written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

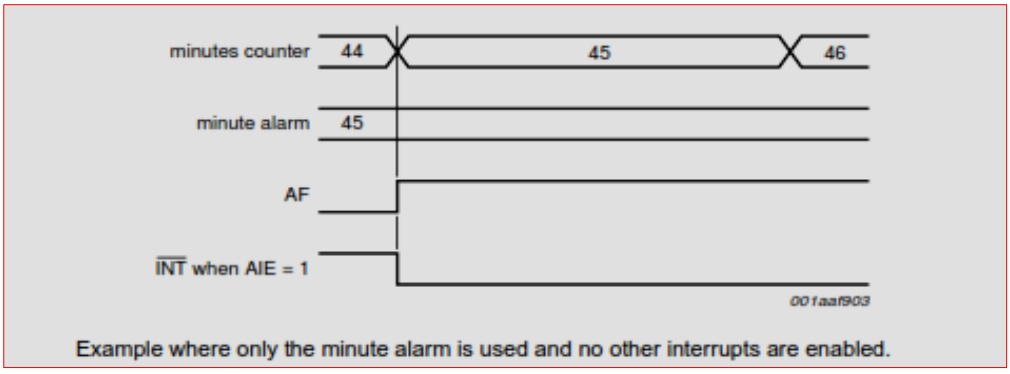


Figure 9, Section 5. Alarm flag timing

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Table 21 Section 5. Flag Location in Register Control 2

Register	Bit							
	7	6	5	4	3	2	1	0
Control 2	WTAF	CTAF	CTBF	SF	AF	-	-	-

Table 22, Section 5. shows what instruction must be sent to clear bit AF. In this example, bit CTAF, CTBF, and bit SF are unaffected.

Table 22 Section 3. Example to Clear Only AF (bit 3)

Register	Bit [1]							
	7	6	5	4	3	2	1	0
Control 2	0	1	1	1	0	-	-	-

[1] The bits labeled as "-" have to be rewritten with the previous values.

5.7.F Alarm Interrupts

Generation of interrupts from the alarm function is controlled via the bit AIE (register Control 1). If AIE is enabled, the INT1 follows the status of bit AF (Register Control 2). Clearing AF immediately clears INT1. No pulse generation is possible for alarm interrupts.

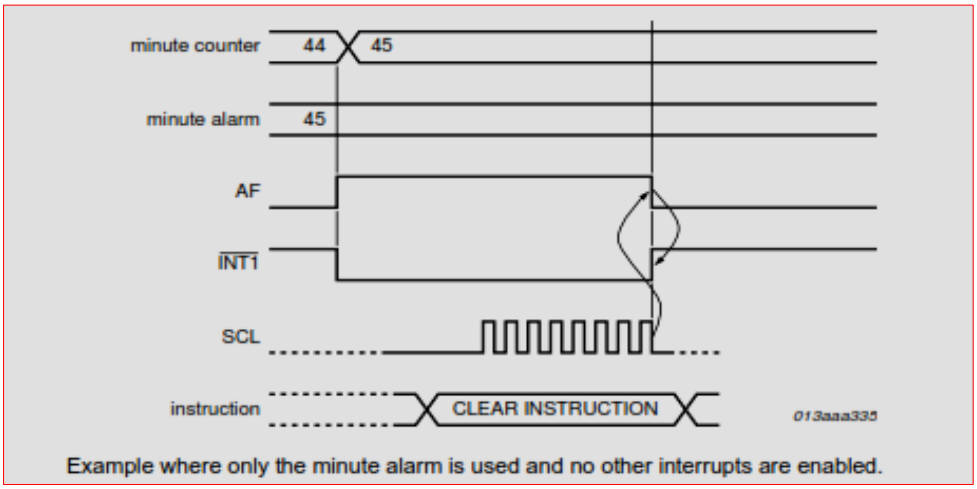


Figure 9, Section 5. Alarm flag timing

5.8 Register Offset

The XXX incorporates an offset register (address 0Eh), which can be used to implement several functions, like:

- Aging adjustment
- Temperature compensation
- Accuracy tuning

Table 23 Section 5. Offset - Offset Register (address 0Eh) Bit Description

Bit	Symbol	Value	Description
7	MODE	0 [1]	offset is made once every two hours
		1 [1]	offset is made once every minute
6 to 0	OFFSET [6:0]	see Table 24, Section 5.	offset value

[1] Default value.

For MODE = 0, each LSB introduces an offset of 4.34ppm. For MODE = 1, each LSB introduces an offset of 4.069ppm. The values of 4.34ppm and 4.069ppm are based on a nominal 32.768kHz clock. The offset value is coded in two's complement giving a range of +63LSB to -64LSB.

Table 24 Section 5. Offset values

OFFSET [6:0]	Offset value in decimal	Offset value in ppm	
		Every two hours (MODE = 0)	Every minute (MODE = 1)
111111	+63	+273.420	+256.347
111110	+62	+269.080	+252.278
:	:	:	:
0000010	+2	+8.680	+8.138
0000001	+1	+4.340	+4.069
0000000	0[1]	0[1]	0[1]
1111111	-1	-4.340	-4.069
1111110	-2	-8.680	-8.138
:	:	:	:
1000001	-63	-273.420	-256.347
1000000	-64	-277.760	-260.416

[1] Default value.

The correction is made by adding or subtracting clock correction pulses, thereby changing the period of a single second.

It is possible to monitor when correction pulses are applied. To enable correction interrupt generation, bit CIE (Register Control 1) has to be set logic 1. At every correction cycle a 1/4096s pulse is generated on pin INTx. If multiple correction pulses are applied, a 1/4096s interrupt pulse is generated for each correction pulse applied.

5.8.A Correction when MODE = 0

The correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values have been implemented.

Table 25, Section 5. Correction pulses for Mode = 0

Correction Value	Hour	Minute	Correction pulses on INT1 per minute [1]
+1 or -1	02	00	1
+2 or -2	02	00 and 01	1
+3 or -3	02	00, 01, and 02	1
:	:	:	:
+59 or -59	02	00 to 58	1
+60 or -60	02	00 to 59	1
+61 or -61	02	00 to 59	1
	03	00	1
+62 or -62	02	00 to 59	1
	03	00 and 01	1
+63 or -63	02	00 to 59	1
	03	00, 01, and 02	1
-64	02	00 to 59	1
	03	00, 01, 02, and 03	1

[1] The correction pulses on pin INT1 are 1/64s wide

In MODE = 0, any timer or clock output using a frequency below 64Hz is affected by the clock correction (see Table 26, Section 5).

Table 26, Section 5. Effect of Clock Correction for MODE = 0

Clockout Frequency (Hz)	Effect of Correction	Timer Source Clock Frequency (Hz)	Effect of Correction
32768	no effect	4096	no effect
16384	no effect	64	no effect
8192	no effect	1	affected
4096	no effect	1/60	affected
1024	no effect	1/3600	affected
32	affected	-	-
1	affected	-	-

5.8.B Correction when MODE = 1

The correction is triggered once per minute and then correction pulses are applied once per second up to a maximum of 60 pulses. When correction values greater than 60 pulses are used, additional correction pulses are made in the 59th second.

Clock correction is made more frequently in MODE = 1; however, this can result in higher power consumption.

Table 27, Section 5. Correction Pulses for MODE = 1

Correction Value	Minute	Second	Correction pulses on INT1 per second [1]
+1 or -1	02	00	1
+2 or -2	02	00 and 01	1
+3 or -3	02	00, 01, and 02	1
:	:	:	:
+59 or -59	02	00 to 58	1
+60 or -60	02	00 to 59	1
+61 or -61	02	00 to 58	1
	02	59	2
+62 or -62	02	00 to 58	1
	02	59	2
+63 or -63	02	00 to 58	1
	02	59	4
-64	02	00 to 58	1
	02	59	5

[1] The correction pulses on pin INTx are 1/4096s wide. For multiple pulses, they are repeated at an interval of 1/2048s.

In MODE = 1, any timer source clock using a frequency below 4.096kHz is also affected by the clock correction (see Table 28, Section 5).

Table 28, Section 5. Effect of Clock Correction for MODE = 1

Clockout Frequency (Hz)	Effect of Correction	Timer Source Clock Frequency (Hz)	Effect of Correction
32768	no effect	4096	no effect
16384	no effect	64	affected
8192	no effect	1	affected
4096	no effect	1/60	affected
1024	no effect	1/3600	affected
32	affected	-	-
1	affected	-	-

5.8.C Offset Calibration Workflow

The calibration offset has to be calculated based on the time. Figure 10, Section 5 shows the workflow how the offset register values can be calculated:

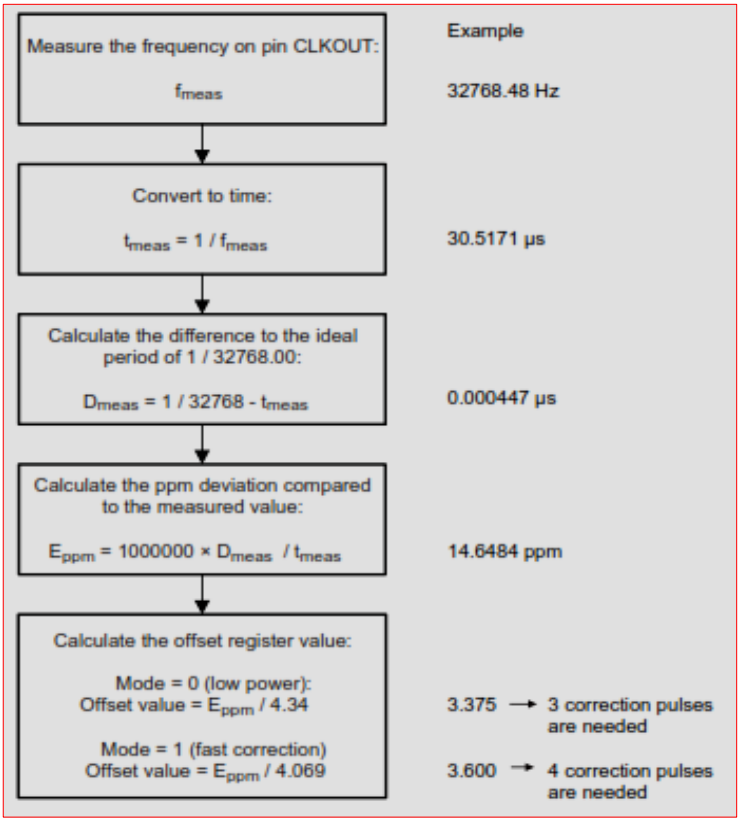


Figure 10, Section 5. Offset calibration calculation workflow

5.9 Timer Function

The XXX has three timers:

- Timer A can be used as a watchdog timer or a countdown timer (see Section 5.9.B). It can be configured by using TAC[1:0] in the Tmr_CLKOUT_ctrl register (0Fh)
- Timer B can be used as a countdown timer (see Section 5.9.C). It can be configured by using TBC in the Tmr_CLKOUT_ctrl register (0Fh)
- Second interrupt timer is used to generate an interrupt once per second (see Section 5.9.D)

Timer A and timer B both have five selectable source clocks allowing for countdown periods from less than 1ms to 255h. To control the timer functions and timer output, the registers 01h, 0Fh, 10h, 11h, 12h, and 13h are used.

5.9.A Timer Register

5.9.A1 Register Tmr_CLKOUT_ctrl and clock output

Table 29, Section 5. Tmr_CLKOUT_ctrl - Timer CLKOUT Control Register (address 0Fh) Bit Description

Bit	Symbol	Value	Description
7	TAM	0 [1]	permanent active interrupt for timer A and for the second interrupt timer
		1	pulsed interrupt for timer A and the second interrupt timer
6	TBM	0 [1]	permanent active interrupt for timer B
		1	pulsed interrupt for timer B
5 to 3	COF [2:0]	see Table 30, Section 5	CLKOUT frequency selection timer A is disabled
2 to 1	TAC [1:0]	00 [1] to 11	
		01	timer A is configured as countdown timer; if CTAIE (register Control 2) is set logic 1, the interrupt is activated when the countdown timed out
		10	timer A is configured as watchdog timer; if WTAIE (register Control 2) is set logic 1, the interrupt is activated when timed out
0	TBC	0 [1]	timer B is disabled
		1	timer B is enabled; if the CTBIE (register Control 2) is set logic 1, the interrupt is activated when countdown timed out

[1] Default value.

5.9.A2 CLKOUT Frequency Selection

Clock output operation is controlled by the COF [2:0] in the Tmr_CLKOUT_ctrl register. Frequencies of 32.768kHz (default) down to 1Hz can be generated (see Table 30, Section 5) for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

A programmable square wave is available at pin INT1/CLKOUT and pin CLKOUT, which are both open-drain outputs. Pin INT1/CLKOUT has both functions of INT1 and CLKOUT combined.

The duty cycle of the selected clock is not controlled but due to the nature of the clock generation, all clock frequencies except 32.768kHz have a duty cycle of 50:50.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the INT1/CLKOUT and CLKOUT pins are high-impedance for all frequencies except for 32.768kHz, 16.384kHz and 8.192kHz. For more details, see Section 5.10.

Table 30, Section 5. CLKOUT Frequency Selection

COF [2:0]	CLKOUT Frequency (Hz)	Typical Duty Cycle [1]	Effect of STOP Bit
000 [2]	32768	60:40 to 40:60	no effect
001	16384	50:50	no effect
010	8192	50:50	no effect
011	4096	50:50	CLKOUT = high-Z
100	1024	50:50	CLKOUT = high-Z
101	32	50:50 [3]	CLKOUT = high-Z
110	1	50:50 [3]	CLKOUT = high-Z
111	CLKOUT disabled (high-Z)		

[1] Duty cycle definition: % HIGH-level time: % LOW-level time.
[2] Default value
[3] Clock frequency may be affected by offset correction.

5.9.A3 Register Tmr_A_freq_ctrl

Table 31, Section 5. Tmr_A_freq_ctrl - Timer A frequency Control Register (address 10h) Bit Description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	TAQ [2:0]	000	source clock for timer A (see Table 35, Section 5)
			4.096kHz
		001	64Hz
		010	1Hz
		011	1/60Hz
		111 [1]	1/3600Hz
		110	
		100	

[1] Default value.

5.9.A4 Register Tmr_A_reg

Table 32, Section 5. Tmr_A_freq_ctrl - Timer A frequency Control Register (address 10h) Bit Description

Bit	Symbol	Value	Description
7 to 0	TIMER_A_VALUE [7:0]	00 to FF	Timer-period in seconds timer period = n/source clock frequency where n is the countdown value.

5.9.A5 Register Tmr_B_freq_ctrl

Table 33, Section 5. Tmr_B_freq_ctrl - Timer B Frequency Control Register (address 12h) Bit Description

Bit	Symbol	Value	Description
7	-	-	unused
6 to 4	TBW [2:0]		low pulse width for pulsed timer B interrupt
		000 [1]	46.875ms
		001	62.500ms
		010	78.125ms
		011	93.750ms
		100	125.000ms
		101	156.250ms
		110	187.500ms
		111	218.750ms
3	-	-	unused
2 to 0	TBQ [2:0]		source clock for timer B (see Table 35, Section 5)
		000	4.096kHz
		001	64Hz
		010	1Hz
		011	1/60Hz
		111 [1]	1/3600Hz
		110	
		100	

[1] Default value.

5.9.A6 Register Tmr_B_reg

Table 34, Section 5. Tmr_B_reg - Timer B Value Register (address 13h) Bit Description

Bit	Symbol	Value	Description
7 to 0	TIMER_B_VALUE [7:0]	00 to FF	Timer-period in seconds timer period = n/source clock frequency where n is the countdown value

5.9.A7 Programmable Timer Characteristics

Table 35, Section 5. Programmable Timer Characteristics

TAQ [2:0] TAQ [2:0]	Timer source clock frequency	Units	Minimum timer-period (n = 1)	Units	Maximum timer-period (n = 255)	Units
000	4.096	kHz	244	µs	62.256	ms
001	64	Hz	15.625	ms	3.984	s
010	1	Hz	1	s	255	s
011	1/60	Hz	1	min	255	min
111	1/3600	Hz	1	hour	255	hour
110						
100						

5.9.B Timer

With the bit field TAC [1:0] in register Tmr_CLKOUT_ctrl (0Fh) Timer A can be configured as a countdown timer (TAC [1:0] = 01) or watchdog timer (TAC [1:0] = 10).

5.9.B1 Watchdog Timer Function

The 3 bits TAQ [2:0] in register Tmr_A_freq_ctrl (10h) determine one of the five source clock frequencies for the watchdog timer: 4.096kHz, 64Hz, 1Hz, 1/60Hz or 1/3600Hz (see Table 31, Section 5).

The generation of interrupts from the watchdog timer is controlled by using WTAIE bit (register Control 2).

When configured as a watchdog timer (TAC[1:0] = 10), the 8-bit timer value in register Tmr_A_reg (11h) determines the watchdog timer-period.

The watchdog timer counts down from value n in register Tmr_A_reg (11h). When the counter reaches 1, the watchdog timer flag WTAF (register Control 2) is set logic 1 on the next rising edge of the timer clock (see Figure 11, Section 5). In that case:

- If WTAIE = 1, an interrupt will be generated
- If WTAIE = 0, no interrupt will be generated

The interrupt generated by the watchdog timer function of timer A may be generated as pulsed signal or a permanently active signal. The TAM bit (register Tmr_CLKOUT_ctrl) is used to control the interrupt generation mode.

The counter does not automatically reload. When loading the counter with any valid value of n, except 0:

- The flag WTAF is reset (WTAF = 0)
- Interrupt is cleared
- The watchdog timer starts

When loading the counter with 0:

- The flag WTAF is reset (WTAF = 0)
- Interrupt is cleared
- The watchdog timer stops

WTAF is read only. A read of the register Control 2 (01h) automatically resets WTAF (WTAF = 0) and clears the interrupt.

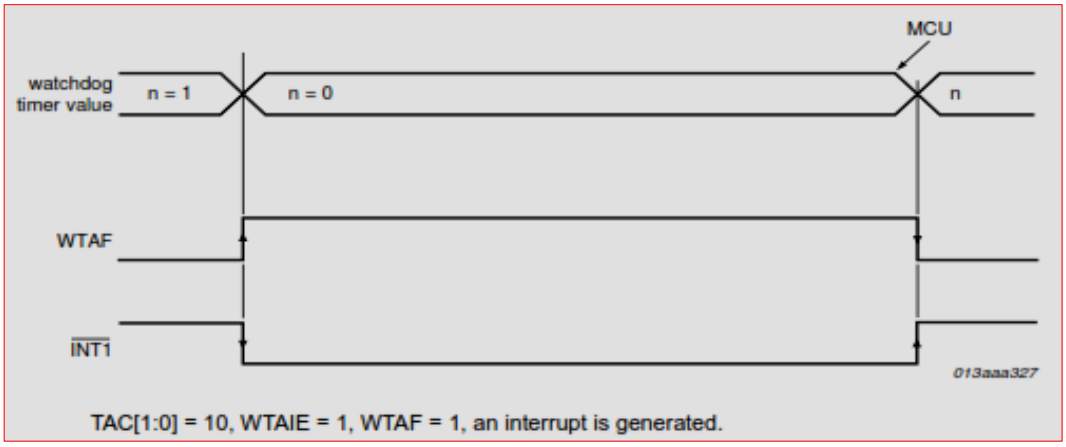


Figure 11, Section 5. Watchdog activates an interrupt when timed out

5.9.B2 Countdown Timer Function

When configured as a countdown timer (TAC [1:0] = 01), timer A counts down from the software programmed 8-bit binary value n in register Tmr_A_reg (11h). When the counter reaches 1, the following events occur on the next rising edge of the timer clock (see Figure 12, Section 5):

- The countdown timer flag CTAF (register Control 2) is set logic 1
- When the interrupt generation is enabled (CTAIE = 1), an interrupt signal on INT1 is generated
- The counter automatically reloads
- The next timer-period starts

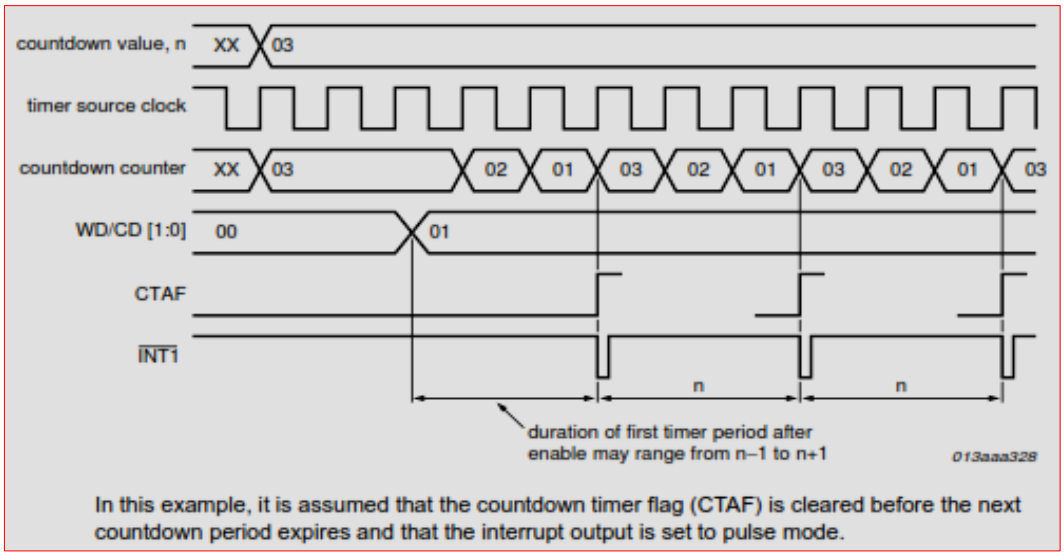


Figure 12, Section 5. General countdown timer behavior

At the end of every countdown, the timer sets the countdown timer flag CTAF (register Control 2). CTAF may only be cleared by using the interface. Instructions, how to clear a flag, are given in Section 5.7.E.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value takes immediate effect. It is not recommended to change n without first disabling the counter by setting TAC[1:0] = 00 (register Tmr_CLKOUT_ctrl). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer-period depends on the chosen source clock; see Table 36, Section 5.

Table 36, Section 5. First Period Delay for Timer Counter Value n

Timer Source Clock	Minimum Timer-period	Maximum Timer-period
4.096kHz	n	n + 1
64Hz	n	n + 1
1Hz	(n-1) + 1/64Hz	n + 1/64Hz
1/60Hz	(n-1) + 1/64Hz	n + 1/64Hz
1/3600Hz	(n-1) + 1/64Hz	n + 1/64Hz

The generation of interrupts from the countdown timer is controlled via the CTAIE bit (register Control 2).

When the interrupt generation is enabled (CTAIE = 1) and the countdown timer flag CTAF is set logic 1, an interrupt signal on INT1 is generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTAF (register Control 2). The TAM bit (register Tmr_CLKOUT_ctrl) is used to control this mode selection. The interrupt output may be disabled with the CTAIE bit (register Control 2).

5.9.C Timer B

Timer B can only be used as a countdown timer and can be switched on and off by the TBC bit in register Tmr_CLKOUT_ctrl (0Fh).

The generation of interrupts from the countdown timer is controlled via the CTBIE bit (register Control 2).

When enabled, it counts down from the software programmed 8 bit binary value n in register Tmr_B_reg (13h). When the counter reaches 1 on the next rising edge of the timer clock, the following events occur (see Figure 13, Section 5):

- The countdown timer flag CTBF (register Control 2) is set logic 1
- When the interrupt generation is enabled (CTBIE = 1), interrupt signals on INT1 and INT2 are generated
- The counter automatically reloads
- The next timer-period starts

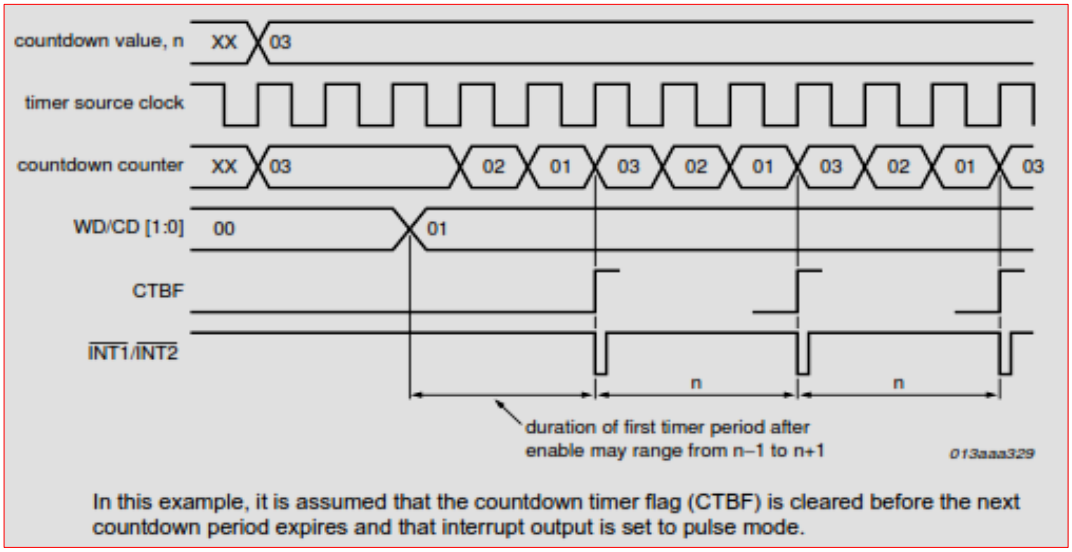


Figure 13, Section 5. General countdown timer behavior

At the end of every countdown, the timer sets the countdown timer flag CTBF (register Control 2). CTBF may only be cleared by using the interface. Instructions, how to clear a flag, are given in Section 5.7.E.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

If a new value of n is written before the end of the actual timer-period, this value will take immediate effect. It is not recommended to change n without first disabling the counter by setting TBC logic 0 (register Tmr_CLKOUT_ctrl). The update of n is asynchronous to the timer clock. Therefore changing it on the fly could result in a corrupted value loaded into the countdown counter. This can result in an undetermined countdown period for the first period. The countdown value n will be correctly stored and correctly loaded on subsequent timer-periods.

Loading the counter with 0 effectively stops the timer.

When starting the countdown timer for the first time, only the first period does not have a fixed duration. The amount of inaccuracy for the first timer-period depends on the chosen source clock; see Table 36, Section 5.

When the interrupt generation is enabled (CTBIE = 1) and the countdown timer flag CTAF is set logic 1, interrupt signal on INT1 is generated. The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal, which follows the condition of CTBF (register Control 2). The TBM bit (register Tmr_CLKOUT_ctrl) is used to control this mode selection. Interrupt output may be disabled with the CTBIE bit (register Control 2).

5.9.D Second Interrupt Timer

XXX has a pre-defined timer, which is used to generate an interrupt once per second. The pulse generator for the second interrupt timer operates from an internal 64Hz clock and generates a pulse of 1/64s in duration. It is independent of the watchdog or countdown timer and can be switched on and off by the SIE bit in register Control 1 (00h).

The interrupt generated by the second interrupt timer may be generated as pulsed signal every second or as a permanently active signal. The TAM bit (register Tmr_CLKOUT_ctrl) is used to control the interrupt generation mode.

When the second interrupt timer is enabled (SIE = 1), then the timer sets the flag SF (register Control 2) every second (see Table 37, Section 5). SF may only be cleared by using the interface. Instructions, how to clear a flag, are given in Section 5.7.E.

Table 37, Section 5. Effect of bit SIE on INT1 and bit SF

SIE	Result on INT1	Result on SF
0	no interrupt generated	SF never set
1	an interrupt once per second	SF set when seconds counter increments

When SF is logic 1:

- If TAM (register Tmr_CLKOUT_ctrl) is logic 1, the interrupt is generated as a pulsed signal every second
- If TAM is logic 0, the interrupt is a permanently active signal that remains, until SF is cleared

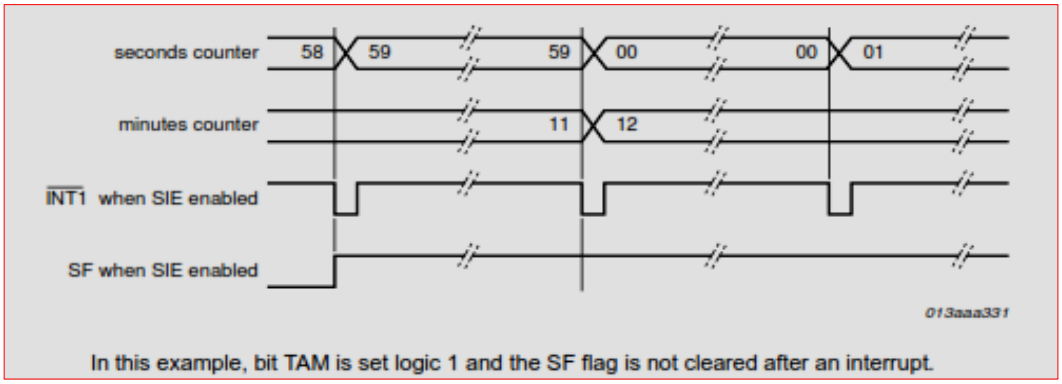


Figure 14, Section 5. Example for second interrupt when TAM = 1

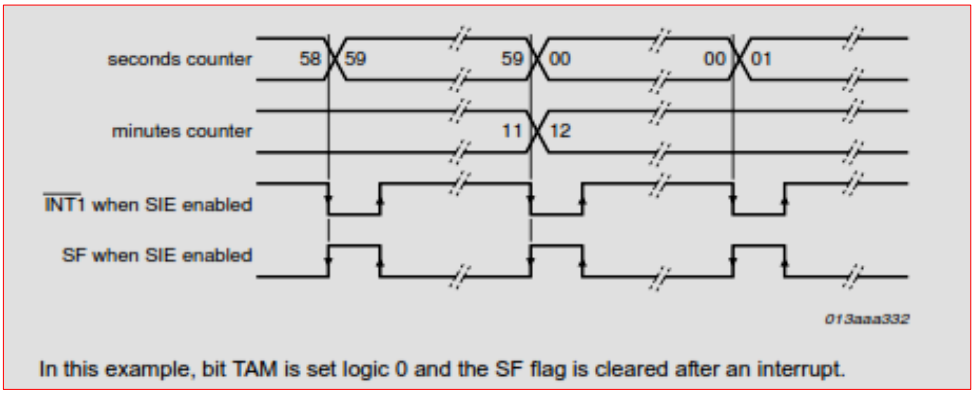


Figure 15, Section 5. Example for second interrupt when TAM = 0

5.9.E Timer Interrupt Pulse

The timer interrupt is generated as a pulsed signal when TAM or TBM are set logic 1. The pulse generator for the timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the timer and on the timer register value n. So, the width of the interrupt pulse varies; see Table 38, Section 5 and Table 39, Section 5.

Table 38, Section 5. Interrupt Low Pulse Width for Timer A
Pulse mode, bit TAM set logic 1.

Source Clock (Hz)	Interrupt Pulse Width	
	n = 1 [1]	n > 1 [1]
4096	122µs	244µs
64	7.812ms	15.625ms
1	15.625ms	15.625ms
1/60	15.625ms	15.625ms
1/3600	15.625ms	15.625ms

[1] n = loaded timer register value. Timer stops when n = 0.

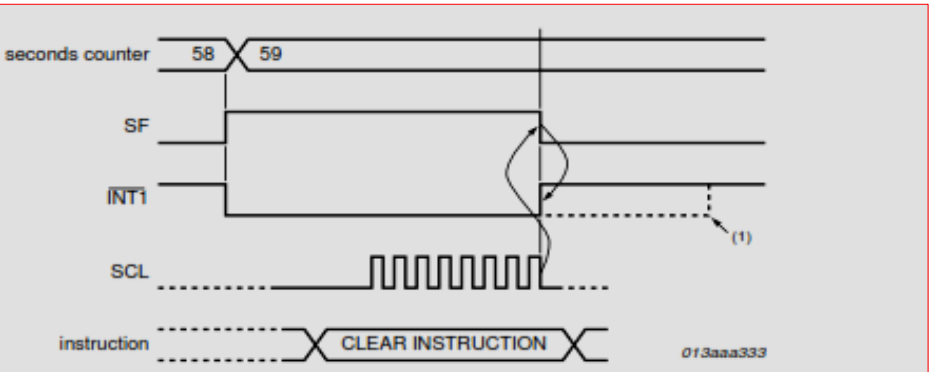
For timer B, interrupt pulse width is programmable via bit TBM (register Tmr_CLKOUT_ctrl).

Table 39, Section 5. Interrupt Low Pulse Width for Timer B
Pulse mode, bit TBM set logic 1.

Source Clock (Hz)	Interrupt Pulse Width	
	n = 1 [1]	n > 1 [1]
4096	122µs	244µs
64	7.812ms	see Table 33, Sec. 3 [2]
1	see Table 33, Sec. 3	:
1/60	:	:
1/3600	:	:

[1] n = loaded timer register value. Timer stops when n = 0.
[2] If pulse period is shorter than the setting via bit TBW [2:0], the interrupt pulse width is set to 15.625ms.

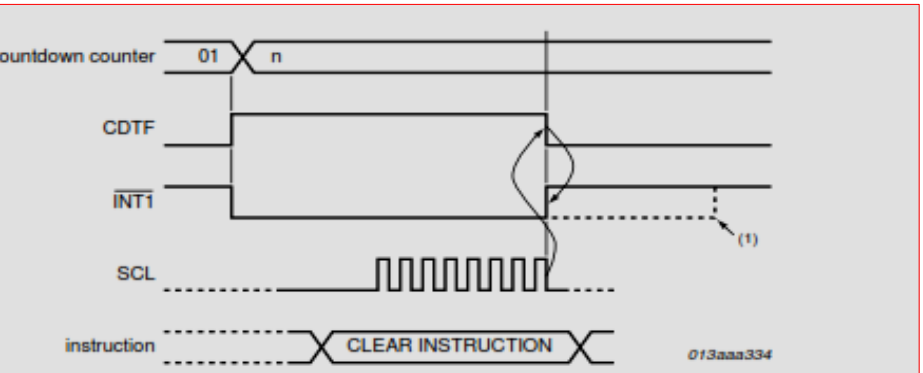
When flags like SF, CTAF, WTAF, and CTBF are cleared before the end of the interrupt pulse, then the interrupt pulse is shortened. This allows the source of a system interrupt to be cleared immediately when it is serviced, that is, the system does not have to wait for the completion of the pulse before continuing; see Figure 16, Section 5 and Figure 17, Section 5. Instructions for clearing flags can be found in Section 5.7.E. Instructions for clearing the bit WTAF can be found in Section 5.9.B1.



(1) Indicates normal duration of $\overline{INT1}$ pulse.

The timing shown for clearing bit SF is also valid for the non-pulsed interrupt mode, that is, when TAM set logic 0, where the $\overline{INT1}$ pulse may be shortened by setting SIE logic 0.

Figure 16, Section 5. Example of shortening the INT1 pulse by clearing the SF flag



(1) Indicates normal duration of $\overline{INT1}$ pulse.

The timing shown for clearing CTAF is also valid for the non-pulsed interrupt mode, that is, when TAM set logic 0, where the $\overline{INT1}$ pulse may be shortened by setting CTAIE logic 0.

Figure 17, Section 5. Example of shortening the INT1 pulse by clearing the CTAF flag

5.10 STOP Bit Function

The STOP bit function allows the accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1Hz ticks are generated. The time circuits can then be set and do not increment until the STOP bit is released (see Figure 18, Section 5).

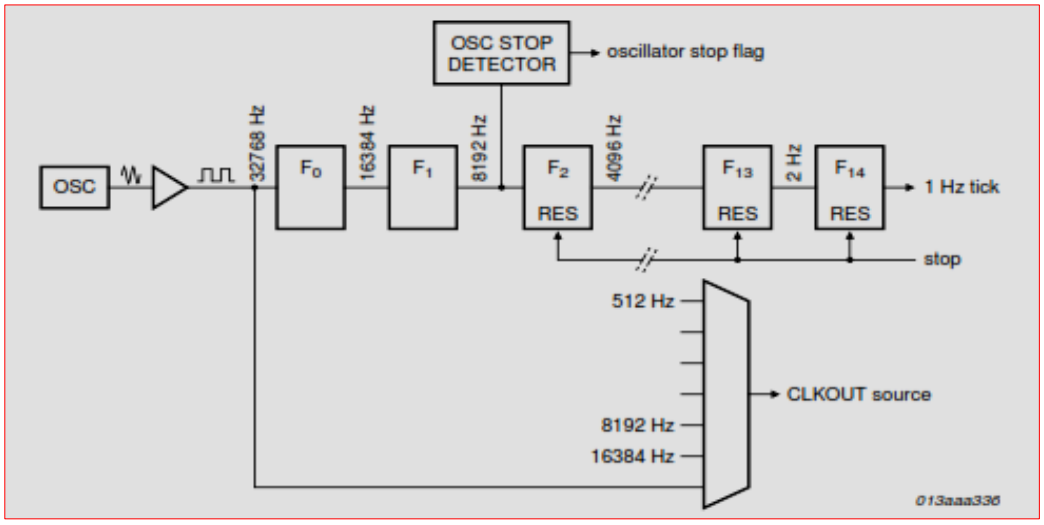


Figure 18, Section 5. STOP Bit

STOP does not affect the output of 32.768kHz or 8.192kHz (see Section 5.9.A1).

The Lower stage of the prescaler (F_0 and F_1) are not reset. And because the I^2C-bus interface is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192kHz cycle (see Figure 19, Section 5).

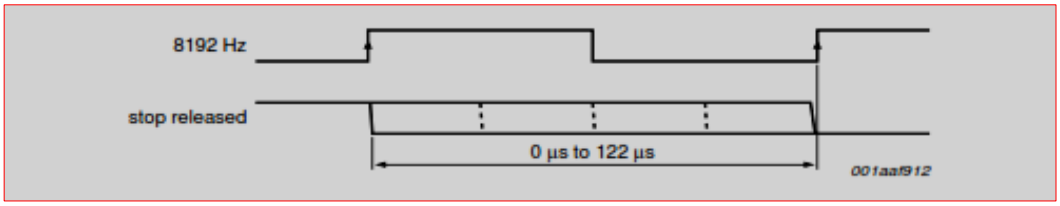
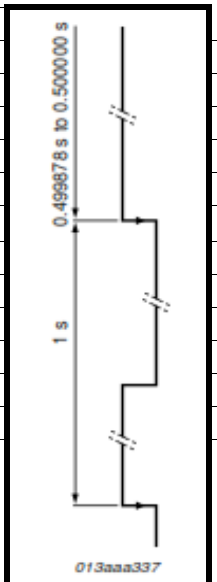


Figure 19, Section 5. STOP Bit Release Timing

The first increment of the time circuits is between 0.499878s and 0.500000s and after STOP is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 40, Section 5).

Table 40, Section 5. First increment of time circuits after STOP release

Bit STOP	Prescaler Bits [1] F_0F_1 - F_2 to F_{14}	1Hz Tick	Time HH:MM:SS	Comment
Clock is running normally				
0	01-0000111010100		12:45:12	prescaler counting normally
STOP is activated by user; F0F1 are not reset and values cannot be predicted externally				
1	XX-0000000000000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0000000000000		08:00:00	prescaler is reset; time circuits are frozen
STOP is released by user				
0	XX-0000000000000		08:00:00	prescaler is now running
0	XX-1000000000000		08:00:00	-
0	XX-0100000000000		08:00:00	-
0	XX-1100000000000		08:00:00	-
:	:		:	:
0	11-1111111111110		08:00:00	-
0	00-0000000000001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
0	10-0000000000001		08:00:01	-
:	:		:	:
0	11-1111111111111		08:00:01	-
0	00-0000000000000		08:00:01	-
:	:		:	:
0	11-1111111111110		08:00:01	-
0	00-0000000000001		08:00:02	0 to 1 transition of F_{14} increments the time circuits

[1] F_0 is clocked at 32.768kHz.

5.11 I2C-Bus Interface

The I^2C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines are connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

5.11.A Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line remains stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as control signals (see Figure 20, Section 5).

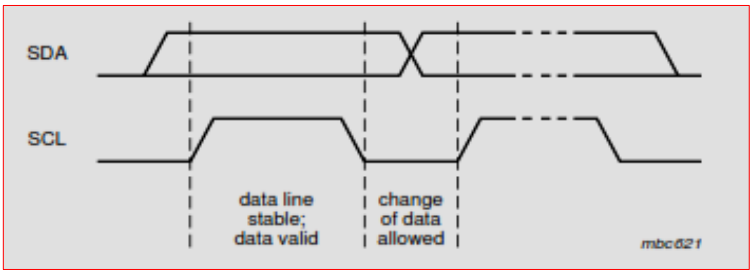


Figure 20, Section 5. Bit Transfer

5.11.B START and STOP Conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line, while the clock is HIGH, is defined as the STOP condition (P) (see Figure 21, Section 5).

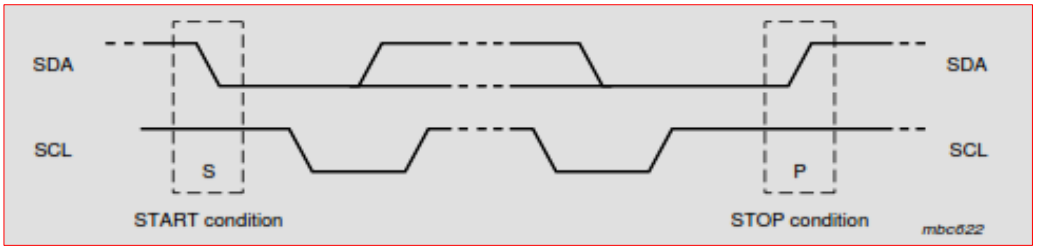


Figure 21, Section 5. Definition of START and STOP Conditions

For this device, a repeated START is not allowed. Therefore, a STOP has to be released before the next START.

5.11.C System Configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master and the devices, which are controlled by the master, are the slaves.

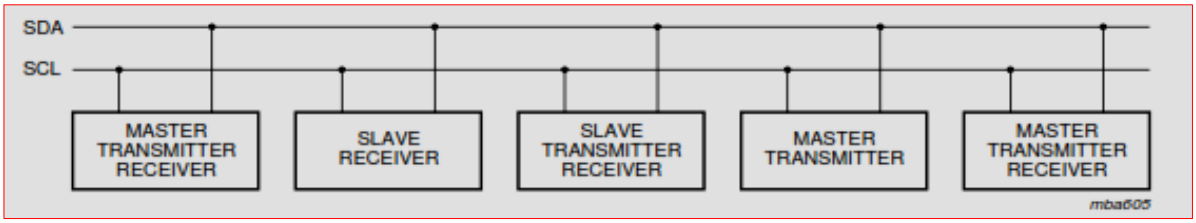


Figure 22, Section 5. System Configuration

The XXX can act as a slave transmitter and a slave receiver.

5.11.D Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge cycle after the reception of each byte
- Also a master receiver must generate an acknowledge cycle after the reception of each byte that has been clocked out of the slave transmitter
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the related acknowledge clock pulse (set-up and hold times must be considered)
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge cycle on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition

Acknowledgement on the I^2C-bus is shown in Figure 23, Section 5.

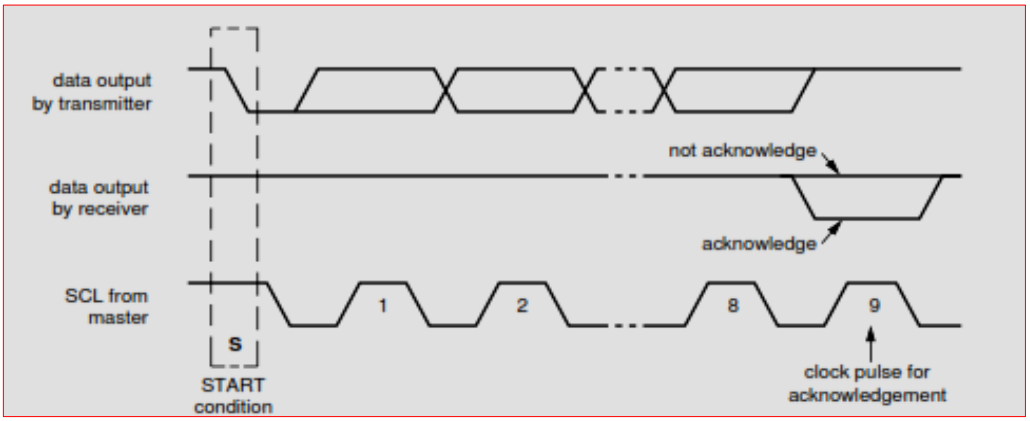


Figure 23, Section 5. Acknowledgement on the I²C-Bus

5.11.E I2C-Bus Protocol

One I²C-bus slave address (1101000) is reserved for the XXX. The entire I²C-bus slave address byte is shown in Table 41, Section 5.

Table 41, Section 5. I²C Slave Address Byte

	Slave Address [1]							
	7	6	5	4	3	2	1	0
Bit	MSB							LSB
	1	1	0	1	0	0	0	R/W

[1] Devices with other I²C-bus slave addresses can be produced on request.

After a START condition, the I²C slave address has to be sent to the XXX device.

The R/W bit defines the direction of the following single or multiple byte data transfer. For the format and the timing of the START condition (S), the STOP condition (P) and the acknowledge bit (A) refer to the I²C-bus characteristics (see Ref. R9). In the write mode, a data transfer is terminated by sending either the STOP condition or the START condition of the next data transfer.

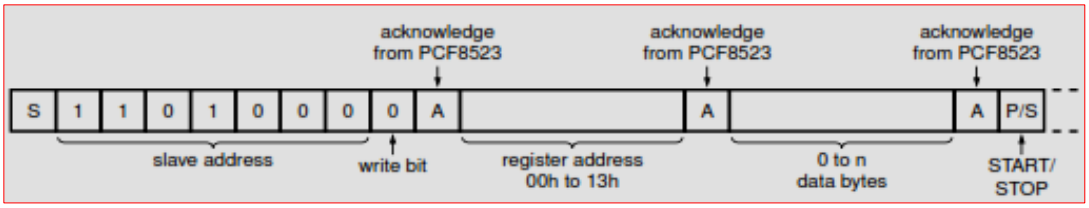


Figure 24, Section 5. Bus protocol for write mode

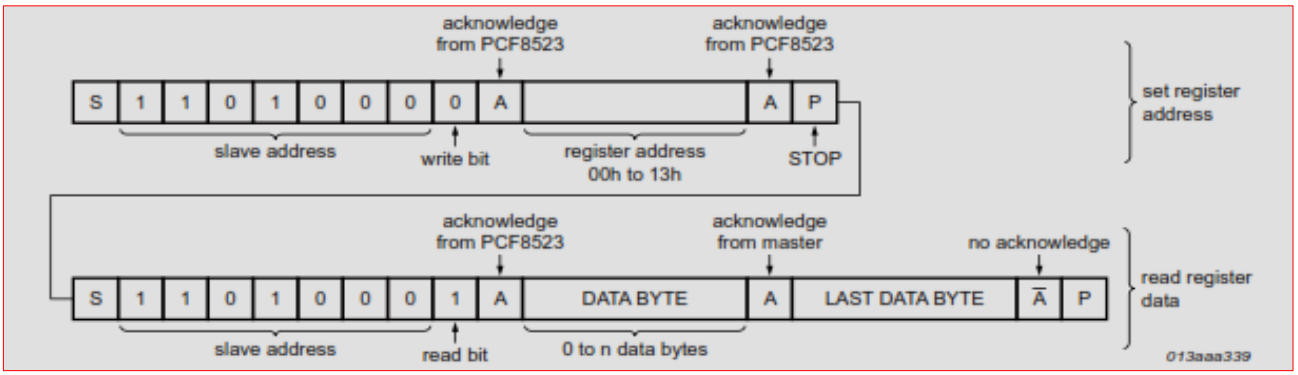


Figure 25, Section 5. Bus protocol for read mode

6. Limiting Values

Table 1, Section 6. Limiting Values

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		-0.5	+6.5	V
I_{DD}	Supply Current		-50	+50	mA
V_I	Input Voltage		-0.5	+6.5	V
V_O	Output Voltage		-0.5	+6.5	V
I_I	Input Current		-10	+10	mA
I_O	Output Current		-10	+10	mA
V_{BAT}	Battery Supply Voltage		-0.5	+6.5	V
P_{tot}	Total Power Dissipation		-	300	mW
V_{ESD}	Electrostatic Discharge Voltage	HBM for all XXX [1]	-	±2000	V
		CDM for all packaged XXX [2]	-	±1500	V
I_{IU}	Latch-up current	[3]	-	100	mA
T_{stg}	Storage Temperature	[4]	-65	+150	°C
T_{amb}	Ambient Temperature	Operating Device	-40	+85	°C

[1] Pass level; Human Body Model (HBM), according to Ref. R4.
[2] Pass level; Charged-Device Model (CDM), according to Ref. R5.
[3] Pass level; latch-up testing according to Ref. R6 at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see Ref. R10) the devices have to be stored at a temperature of +8°C to +45°C and a humidity of 25 % to 75 %.

7. Static Characteristics

Table 1, Section 7. Static Characteristics

V_{DD} = 1.2V to 5.5V; V_{SS} = 0V; T_{amb} = -40°C to +85°C; f_{OSC} = 32.768kHz; quartz R_s = 40kΩ; C_L = 7pF; unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supplies						
V_{DD}	Supply Voltage	I^2C-bus inactive; for clock data integrity				
		T_{amb} = -40°C to +85°C [1]	1.2	3.3	4	V
		T_{amb} = +10°C to +85°C [2]	1.0	3.3	4	V
		I^2C-bus active	1.6	3.3	4	V
		power management function active of V_{DD}	1.8	-	3.3	V
SR	Slew Rate		-	-	±0.5	V/ms
I_{DD}	Supply Current	I^2C-bus active; f_{SCL} = 1000kHz	-	-	200	µA
		I^2C-bus inactive (f_{SCL} = 0Hz); interrupts disabled				
		Clock-out disabled; power management function disabled (PM [2:0] = 111)				
		T_{amb} = 25°C; V_{DD} = 3.0V [3]	-	150	-	nA
		T_{amb} = -40°C to +85°C; V_{DD} = 2.0V to 5.0V [3]	-	-	500	nA
		Clock-out enabled at 32kHz; power management function enabled (PM [2:0] = 000)				
		T_{amb} = 25°C; V_{BAT} or V_{DD} = 3.0V [4]	-	1200	-	nA
		T_{amb} = -40°C to +85°C; V_{BAT} or V_{DD} = 2.0V to 5.0V [4]	-	-	3600	nA
$I_{L(bat)}$	Battery Leakage Current	V_{DD} active; V_{BAT} = 3.0V	-	50	100	nA
Power Management						
$V_{th(sw)bat}$	Battery Switch Threshold Voltage		2.28	2.5	2.7	V
Inputs [5]						
V_{IL}	LOW-level Input Voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level Input Voltage		$0.7V_{DD}$	-	-	V
V_I	Input Voltage		-0.5	-	V_{DD} + 0.5	V
I_{LI}	Input Leakage Current	VI = VSS or VDD	-	0	-	nA
		Post ESD Event	-1	-	+1	µA
C_I	Input Capacitance	[6]	-	-	7	pF

Table 1, Section 7. Static Characteristics *...continued*

V_{DD} = 1.2V to 5.5V; V_{SS} = 0V; T_{amb} = -40°C to +85°C; f_{OSC} = 32.768kHz; quartz R_s = 40kΩ; C_L = 7pF; unless otherwise specified.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Outputs						
V_O	Output Voltage	on pins INT1/CLKOUT, CLKOUT, SDA (refers to external pull-up voltage)	-0.5	-	3.3	V
V_{OL}	LOW-level Output Voltage		V_{SS}	-	0.4	V
I_{OL}	LOW-level Output Current	output sink current; on pins INT1/CLKOUT, CLKOUT, V_{OL} = 0.4V; V_{DD} = 5V [7]	1.5	-	-	mA
		on pin SDA V_{OL} = 0.4V; V_{DD} = 3.0V [7]	20	-	-	mA
ILO	Output Leakage Current	$V_O = V_{SS}$ or V_{DD}	-	0	-	nA
		Post ESD event	-1	-	+1	µA

[1] For reliable oscillator start at power-up: $V_{DD} = V_{DD}(min) + 0.3V$.
[2] For reliable oscillator start at power-up: $V_{DD} = V_{DD}(min) + 0.5V$.
[3] Timer source clock = 1/3600Hz, level of pins SCL and SDA is V_{DD} or V_{SS}.
[4] When the device is supplied via the V_{BAT} pin instead of the V_{DD} pin, the current values for I_{BAT} will be as specified for I_{DD} under the same condition.
[5] The I^2C-bus is 5V tolerant.
[6] Implicit by design.
[7] Tested on sample basis.
[8] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = (C_{OSCI} * C_{OSCO})/(C_{OSCI} + C_{OSCO})$.
[9] Tested at 25°C.
[10] Crystal characteristic specification.

8. Dynamic Characteristics

Table 1, Section 8. I²C-Bus Interface Timing

All timing characteristics are valid within the operating supply voltage and ambient temperature range and reference to 30% and 70% with an input voltage swing of V_{SS} to V_{DD} (see Figure 1, Section 8).

Symbol	Parameter	Condition	Standard Mode		Fast Mode (FM)		Fast Mode Plus (FM+)[1]		Unit
			Min	Max	Min	Max	Min	Max	
Pin SCL									
f_{SCL}	SCL clock frequency	[2]	-	100	-	400	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	-	4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	LOW period of the SCL clock	-	4.0	-	0.6	-	0.26	-	µs
Pin SDA									
$t_{SU;DAT}$	Data Set-up Time	-	250	-	100	-	50	-	ns
$t_{HD;DAT}$	Data Hold Time	-	0	-	0	-	0	-	ns
Pins SCL and SDA									
t_{BUF}	Bus free time between a STOP and START condition	-	4.7	-	1.3	-	0.5	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	-	4.0	-	0.6	-	0.26	-	µs
$t_{HD;STA}$	Hold time (repeated) START condition	-	4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	Set-up time (repeated) START condition	-	4.7	-	0.6	-	0.26	-	µs
t_r	Rise time of both SDA and SCL signals	[3][4]	-	1000	$20 + 0.1C_b$	300	-	120	ns
t_f	Fall time of both SDA and SCL signals	[3][4]	-	300	$20 + 0.1C_b$	300	-	120	ns
C_b	Capacitive load for each bus line		-	400	-	400	-	550	pF
$t_{VD;ACK}$	Data valid acknowledge time	[5]	-	3.45	-	0.9	-	0.45	µs
$t_{VD;DAT}$	Data valid time	[6]	-	3.45	-	0.9	-	0.45	µs
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns

[1] Fast mode plus guaranteed at $3.0V < V_{DD} < 5.5V$.
[2] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25ms. The bus time-out feature must be disabled for DC operation.
[3] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
[4] The maximum t_f for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin and the SDA/SCL bus lines without exceeding the maximum t_f.
[5] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.
[6] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.
[7] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.

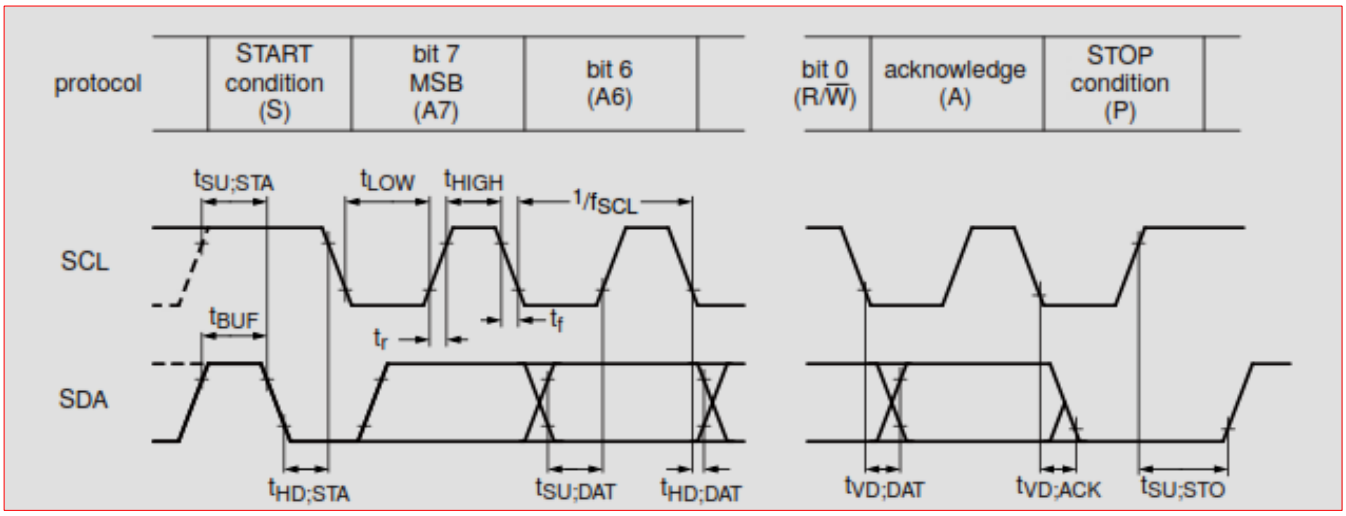


Figure 1, Section 8. I²C-bus timing diagram; rise and fall times refer to 30% and 70%

9. Soldering of SMD Package

This text provides a very brief insight into a complex technology. Refer to *"Recommended Solder Profile for Cardinal Components, Inc."* on Section 10.

9.1 Introducing to Soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

9.2 Wave and Reflow Soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

9.3 Wave Soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

9.4 Reflow Soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 1, Section 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 1, Section 9 and Table 2, Section 9.

Table 1, Section 9. SnPb Eutectic Process (from J-STD-020C)

Package Thickness (mm)	Package Reflow Temperature (°C) Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 2, Section 9. Lead-Free Process (from J-STD-020C)

Package Thickness (mm)	Package Reflow Temperature (°C) Volume (mm^3)		
	< 350	≥ 350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, (see Figure 1, Section 9).

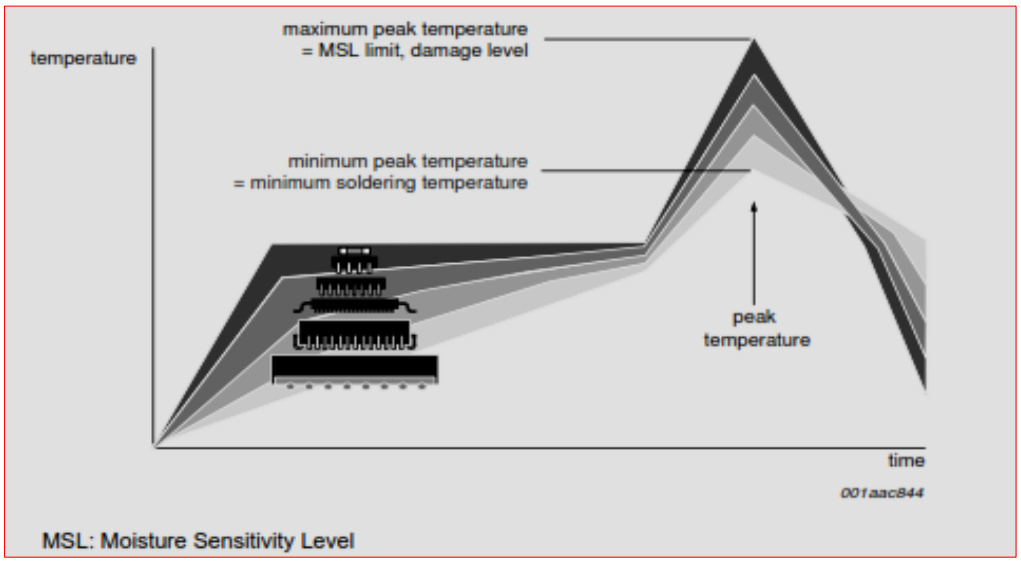


Figure 1, Section 9. Temperature Profiles for Large and Small Components

For further information on temperature profiles, refer to *"Recommended Solder Profile for Cardinal Components, Inc."* on Section 10.

10. Recommended Solder Profile for Cardinal Components, Inc.

Recommended Solder Profile for Cardinal Components, Inc. in fared reflow. Do not use ultrasonic-wave soldering or wave solder with package immersed in solder.

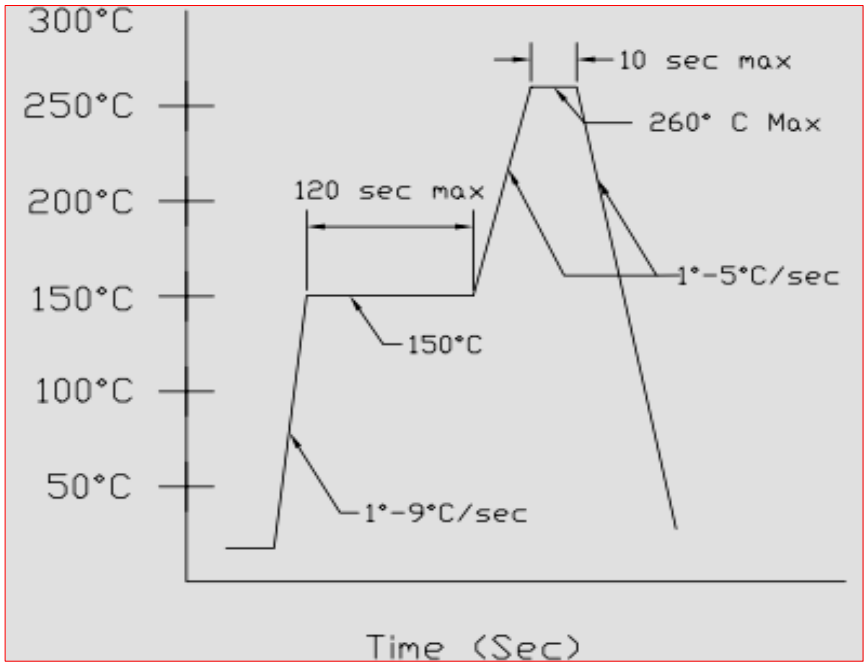


Figure 1, Section 10. Recommended Solder Profile

11. References

[R1] **IEC 60134** — Rating systems for electronic tubes and valves and analogous semiconductor devices
[R2] **IEC 61340-5** — Protection of electronic devices from electrostatic phenomena
[R3] **IPC/JEDEC J-STD-020D** — Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
[R4] **JESD22-A114** — Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
[R5] **JESD22-C101** — Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Component
[R6] **JESD78** — IC Latch-Up Test
[R7] **JESD625-A** — Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
[R8] **SNV-FA-01-02** — Marking Formats Integrated Circuits
[R9] **UM10204** — I^2C-bus specification and user manual
[R10] **UM10569** — Store and transport requirements

12. Abbreviations

Table 1, Section 12. Abbreviations

Acronym	Description
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
FFC	Film Frame Carrier
HBM	Human Body Metal
I^2C	Inter Integrated Circuit Bus
IC	Integrated Circuit
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed Circuit Board
PM	Post Meridiem
POR	Power On Reset
RTC	Real Time Clock
SCL	Serial Clock Line
SDA	Serial Data Line
SMD	Surface Mount Device
SR	Slew Rate