Series CRTCP

Part Number: CRTCP-A12

Real-Time Clock, Calendar with EnerChip™ Battery and 12µAh Integrated Power Management

1. Features

- Power Manager with Charge Control
- Integrated 12µAh Solid State Battery
- Built-in Energy Storage Protection
- Temperature Compensated Charge Control
- Adjustable Switchover Voltage
- Charges EnerChip™ Over a Wide Supply Range
- Low Standby Power
- SMT - Lead-Free Reflow Tolerant
- Thousands of Recharge Cycles
- Low Self-Discharge
- Eco-Friendly, RoHS Compliant – tested
- Provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.0V to 3.3V
- Ultra-low supply current
  14 nA with RC oscillator
  50 nA with crystal oscillator
- 2 line bidirectional 1MHz Fast-mode Plus (Fm+) I^2C interface, read D1h, write D2h
- Battery backup and switch-over circuit
- Freely programmable timer and alarm with interrupt capability
- Internal Power-On Reset (POR)
- Open-drain interrupt or clock output pins
- Programmable offset register for frequency adjustment

2. Applications

- Smart cards
- Wireless sensors and RFID tags
- Medical electronics
- Consumer appliances
- Business and industrial systems
- Energy harvesting
- Time keeping application
- Battery powered devices
- Metering
- Telemedicine
- Handsets
- Smart energy
- Security camera
- Military surveillance
- Data logging

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3. General Description

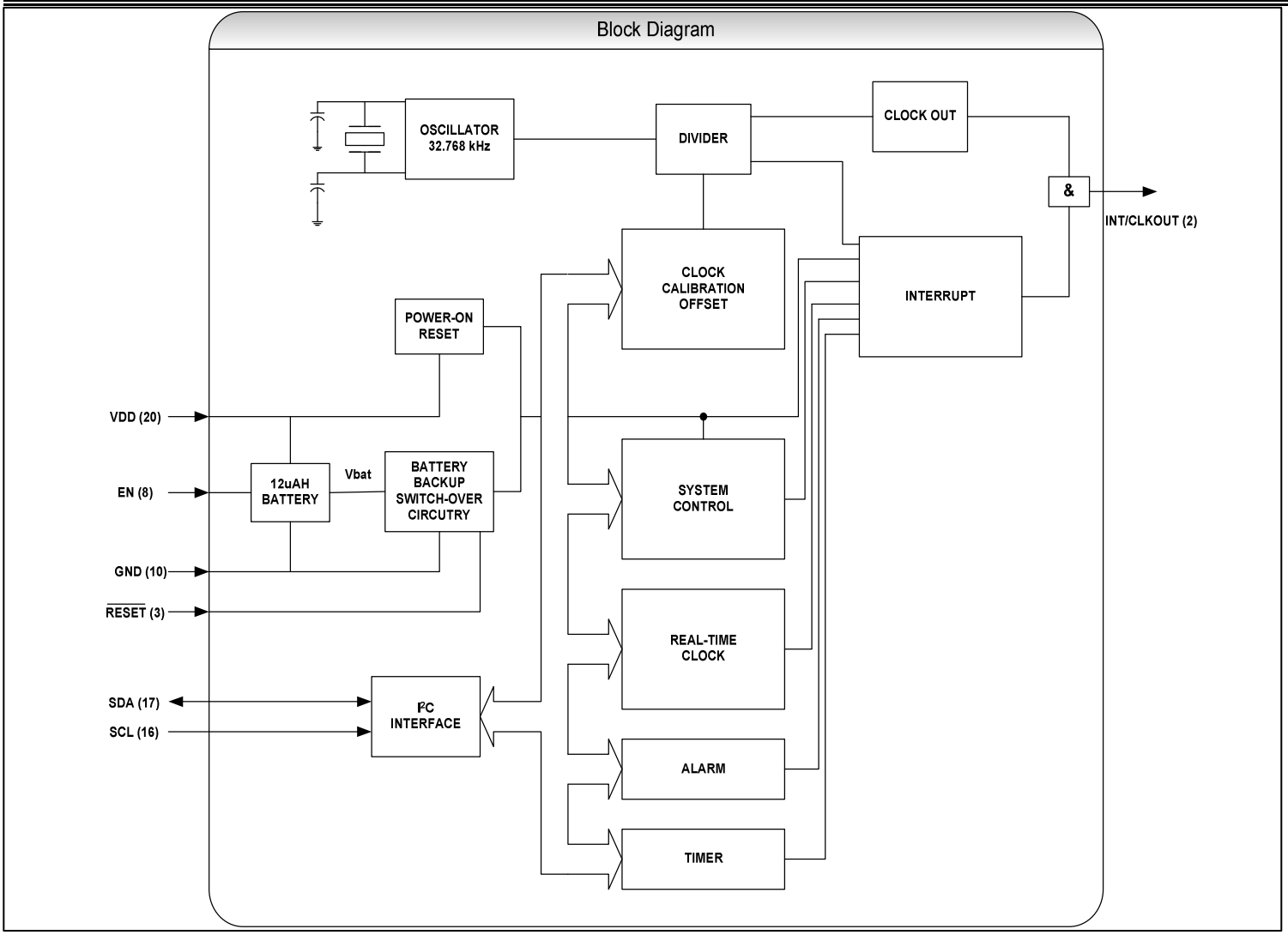
The EnerChip™ CC is the world's first Intelligent Thin Film Energy Storage Device. It is an integrated solution that provides backup energy storage and power management for systems requiring power bridging and/or secondary power.

During normal operation, the EnerChip™ CC charges itself with a controlled voltage using an internal charge pump that operates from 2.5V to 3.3V. An ENABLE pin allows for activation and deactivation of the charge pump using an external control line in order to minimize current consumption and take advantage of the fast recharge time of the EnerChip™.

When the primary power supply dips below a user defined threshold voltage, the EnerChip™ CC will signal this event and route the EnerChip™ voltage to V_{OUT}. The EnerChip™ CC also has energy storage protection circuitry to enable thousands of recharge cycles.

The CRTCP-A12 is a Real-Time Clock (RTC) and calendar optimized for low power consumption. Data is transferred serially via an I^2C-bus with a maximum data rate of 1000kbits/s. Alarm and time functions are available with the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine-tuning of the clock. The CRTCP-A12 has a backup battery switch-over circuit, which detects power failures and automatically switches to the battery supply when a power failure occurs.

4. Block Diagram



5. Functional Description

The CRTCP-A12 contains:

- Time and Date Registers
- Alarm Registers
- Configuration Registers
- An on-chip 32.768kHz oscillator with two integrated load capacitors
- A frequency divider, which provides that source clock for the Real-Time Clock (RTC)
- A programmable clock output
- A 1Mbit/s I^2C-bus interface
- An offset register, which allows fine-tuning of the clock

5.1 Registers Overview

All registers are designed as addressable 8-bit registers although not all bits are implemented.

- The addresses 00h through 07h are used as counters for the clock function (seconds up to years)
- Addresses 08h through 0Eh define the alarm condition
- Addresses 10h and 11h are control registers
- Addresses 12h and 13h are used for interrupt and SQW out control
- Addresses 14h through 16h defines the offset calibration
- Addresses 17h defines the sleep control
- Addresses 18h through 1Ah are used for the timers

The registers Seconds, Minutes, Hours, Days, Weekends, Months, and Years are all coded in Binary Coded Decimal (BCD) format. Other registers are either bit-wise or standard binary. When one of the RTC registers is read, the contents of all counters are frozen. Therefore, faulty reading of the clock and calendar during a carry condition is prevented.

The battery switch-over circuit monitors the main power supply and switches automatically to the backup battery when a power failure condition is detected. Accurate timekeeping is maintained even when the main power supply is interrupted.

Time, Date, Alarm and Status Registers

Address	Register Name	Bit 7	6	5	4	3	2	1	0
Time and Date Registers									
00h	Hundredths	Seconds - Tenths				Seconds - Hundredths			
01h	Seconds	GP0	Seconds - Tens			Seconds - Ones			
02h	Minutes	GP1	Minutes - Tens			Minutes - Ones			
03h	Hours (24 hr)	GP3	GP2	Hours - Tens		Hours - Ones			
03h	Hours (12 hr)	GP3	GP2	AM/ PM	Hours - Tens	Hours - Ones			
04h	Date	GP5	GP4	Date - Tens		Date - Ones			
05h	Months	GP8	GP7	GP6	Month - Tens	Month - Ones			
06h	Years	Years - Tens				Years - Ones			
07h	Weekdays	GP13	GP12	GP11	GP10	GP9	Weekdays		
Alarm Registers									
08h	Hundreths/ Alarm	Hundredths - Alarm - Tenths				Hundredths - Alarm - Hundredths			
09h	Second Alarm	GP14	Second - Alarm - Tens			Second - Alarm - Ones			
0Ah	Minute_Alarm	GP15	Minute - Alarm - Tens			Minute - Alarm - Ones			
0Bh	Hour_Alarm (24 hour)	GP17	GP16	Hour - Alarm - Tens		Hour - Alarm - Ones			
0Bh	Hour_Alarm (12 hour)	GP3	GP2	AM/ PM		Hour - Alarm - Tens			
0Ch	Date_Alarm	GP19	GP18	Date - Alarm - Tens		Date - Alarm - Ones			
0Dh	Month/Alarm	GP22	GP21	GP20	Month/ Alarm - Tens	Month - Alarm - Ones			
0Eh	Weekday/ Alarm	GP27	GP26	GP25	GP24	GP23	Weekday - Alarm		
Status Register									
0Fh	Status	CB	BAT	WDT	BL	TIM	ALM	EX2	EX1

5.2 Control Registers

Address	Register Name	Bit 7	6	5	4	3	2	1	0
10h	Control 1	STOP	12/24	OUTB	OUT	RSP	ARST	PWR2	WRTC
11h	Control 2	OUTPP	-	RS1E	OUT2S			OUT1S	
12h	IntMask	CEB	IM		BLIE	TIE	AIE	EX2E	EX1E
13h	SQW	SQWE	-		SQFS				
14h	Cal_XT	CMDX	OFFSETX						
15h	Cal_RC_Hi	CMDR		OFFSETR[13:8]					
16h	Cal_RC_Low	OFFSETR[7:0]							
17h	Sleep Cntl	SLP	SLRES	EX2P	EX1P	SLST	SLTO		
18h	Timer Cntl	TE	TM	TRPT	RPT			TFS	
19h	Timer	Countdown Timer							
1Ah	Timer Initial	Timer Initial Value							
1Bh	WDT	WDS	BMB						
1Ch	Osc Control	OSEL	ACAL		AOS	FOS	PWGT	OFIE	ACIE
1Dh	Osc Status	XTCAL		LKO2	OMODE	XTF	-	OF	ACF
1Eh	RESERVED	RESERVED							
1Fh	Config Key	Configuration Key							
20h	Trickle	TCS				DIODE		ROUT	
21h	BREF Cntl	BREF				-			
22h	RESERVED	RESERVED							
23h	RESERVED	RESERVED							
24h	RESERVED	RESERVED							
25h	RESERVED	RESERVED							
26h	RESERVED	RESERVED							
27h	RESERVED	RESERVED							
28h	RESERVED	RESERVED							
29h	RESERVED	RESERVED							
2Ah	RESERVED	RESERVED							
2Bh	RESERVED	RESERVED							
2Ch	RESERVED	RESERVED							
2Dh	RESERVED	RESERVED							
2Eh	RESERVED	RESERVED							
2Fh	ASTAT	BBOD	BMIN	-	-	-	-	VINIT	-
30h	OCTRL	WDBM	EXBM	WDDS	EXDS	RSEN	O4EN	O3EN	O1EN
3Fh	Ext Address	O4BM	BPOL	WDIN	EXIN	XEN	XADA	XADS	
40h-7Fh	RAM	Normal RAM Data							
80h-FFh	RAM	Alternate RAM Data							

6. Register Descriptions

Registers are accessed by selecting a register address and then performing read or write operations. Multiple reads or writes may be executed in a single access, with the address automatically incrementing after each byte. The GPx bits are register bits which may be used for general purpose storage. All GPx bits are cleared when the RTC powers up.

6.1 Time and Date Registers

6.1.1 00 - Hundredths (Reset Value = 0x99)

This Register holds the count of hundredths of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 – 99. Note that in order to divide from 32 kHz, the hundredths register will not be fully accurate at all times but will be correct every 500 ms. Maximum jitter of this register will be less that 1 ms. The hundredths Counter is not valid if the 128 Hz RC Oscillator is selected.

6.1.2 01 - Seconds (Reset Value = 0x00)

This register holds the count of seconds, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

6.1.3 02 - Minutes (Reset Value = 0x00)

This register holds the count of minutes, in two binary coded decimal (BCD) digits. Values will be from 00 to 59.

6.1.4 03 - Hours (Reset Value = 0x00)

This register holds the count of hours, in two binary coded decimal (BCD) digits. Values will be from 00 to 23 if the 12/24 bit is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours, and hour values will range from 1 to 12.

6.1.5 04 - Date (Reset Value = 0x01)

This register holds the current day of the month, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

6.1.6 05 - Months (Reset Value = 0x01)

This register holds the current month, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

6.1.7 06 - Years (Reset Value = 0x00)

This register holds the current year, in two binary coded decimal (BCD) digits. Values will range from 00 to 99.

6.1.8 07 - Weekday (Reset Value = 0x00)

This register holds the current day of the week. Values will range from 0 to 6.

6.2 Alarm Registers

6.2.1 08 - Hundredths Alarm (Reset Value = 0x00)

This register holds the alarm value for hundredths of seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

6.2.2 09 - Seconds Alarm (Reset Value = 0x00)

This register holds the alarm value for seconds, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

6.2.3 0A - Minutes Alarm (Reset Value = 0x00)

This register holds the alarm value for minutes, in two binary coded decimal (BCD) digits. Values will range from 00 to 59.

6.2.4 0B - Hours Alarm (Reset Value = 0x00)

This register holds the alarm value for hours, in two binary coded decimal (BCD) digits. Values will range from 00 to 23 if the 12/24 bit is clear. If the 12/24 bit is set, the AM/PM bit will be 0 for AM hours and 1 for PM hours and hour values will be from 1 to 12.

6.2.5 0C - Date Alarm (Reset Value = 0x00)

This register holds the alarm value for the date, in two binary coded decimal (BCD) digits. Values will range from 01 to 31. Leap years are correctly handled from 1900 to 2199.

6.2.6 0D - Months Alarm (Reset Value = 0x00)

This register holds the alarm value for months, in two binary coded decimal (BCD) digits. Values will range from 01 to 12.

6.2.7 0E - Weekday Alarm (Reset Value = 0x00)

This register holds the alarm value for the day of the week. Values will range from 0 to 6.

6.3 Configuration Registers

6.3.1 0F - Status

This register holds a variety of status bits. The register may be written at any time to clear or set any status flag. If the ARST bit is set, any read of the Status Register will clear all of the bits except CB.

CB[7] – Century. This bit will be toggled when the year's register rolls over from 99 to 00 if the CEB bit is a 1. A 0 assumes the century is 19xx or 21xx, and a 1 assumes it is 20xx for leap year calculations.

BAT[6] – set when the system switches to the VBAT Power state.

BAT[5] – set when the Watchdog Timer is enabled and is triggered, and the WDS bit is 0.

BL[4] – set if the battery voltage VBAT crosses the reference voltage selected by BREF in the direction selected by BPOL.

Tim[3] – set when the countdown timer is enabled and reaches zero.

ALM[2] – set when the Alarm function is enabled and all selected Alarm registers match their respective counters.

EX2[1] – set when an external trigger is detected on the WDI pin. The EX2E bit must be set in order for this interrupt to occur, but subsequently clearing EX2E will not automatically clear this flag

EX1[0] – set when an external trigger is detected on ghe EXT1 pin. The EX1E bit must be set in order for this interrupt to occur, but subsequently clearing EX1E will not automatically clear this flag.

6.3.2 10 - Control1 (Reset Value = 0x13)

This register holds some major control signals.

STOP[7] – when 1, stops the oscillator. This bit allows the oscillator to be precisely started, by setting it to 1 and back to 0. The clock is guaranteed to start within one second.

12/24[6] – when 0, the Hours register operates in 24 hour mode. When 1, the Hours register operates in 12 hour mode.

OUTB[5] – a static value which may be driven on the PSW/nIRQ2 pin. The OUTB bit cannot be set to 1 if the LKO2 bit is 1.

OUT[4] – a static value which may be driven on the FOUT/nIRQ pin. This bit also defines the default value for the Square Wave output when SQWE is not asserted.

RSP[3] – Reset Polarity. When 1, the nRST pin is asserted high. When 0, the nRST pin is asserted low.

ARST[2] – auto reset enable. When 1, a read of the Status register will cause any interrupt bits)TIM, BL,ALM, WDT, XT1, XT2) to be cleared. When 0, the bits must be explicitly cleared by writing the Status resister.

PWR2[1] – when 1, the PSW/nIRQ2 pin is driven by a approximately 1 Ω pulldown which allows the RTC to switch power to other system devices through this pin. When 0, the PSW/nIRQ2 pin is a normal open drain output.

WRTC[0] – write RTC. This bit must be set in order to write any of the Counter registers (Hundredths, Seconds, Minutes, Hours, Date, Months, Years or Weekdays).

6.3.3 11 - Control2 (Reset Value = 0x3C)

This register holds additional control and configuration signals for the flexible output pins FOUT/nIRQ and PSW/nIRQ2. Note that POW/nIRQ2 is an open drain output, and FOUT/nIRQ is open drain if OUTPP is 0 and push-pull is OUTPP is 1.

OUTPP[7] – if 1, the FOUT/nIRQ and nTIRQ are push-pull. If 0 these outputs are open drain

RS1E[5] – when 1, enable the nEXTR pin to generate nRST.

OUT2S[4:2] – controls the function of the PSW/nIRQ2 pin as shown.

OUT1S[1:0] – controls the function of the FOUT/nIRQ pin as shown.

PSW/nIRQ2 Pin Control

Out2S Value	PSW/nIRQ2 Pin Function
000	nIRQ if at least one interrupt is enabled, else OUTB
001	SQW if SQWE = 1, else OUTB
010	RESERVED
011	nAIRQ if AIE is set, else OUTB
100	TIRQ if TIE is set, else OUTB
101	nTIRQ if TIE is set, else OUTB
110	SLEEP
111	OUTB

FOUT/nIRQ Pin Function

OUTS Value	FOUT/nIRQ Pin Function
00	nIRQ if at least one interrupt is enabled, else OUT
01	SQW if SQWE = 1, else OUT
10	SQW if SQWE = 1, else nIRQ if at least one interrupt is enabled, else OUT
11	nAIRQ if AIE is set, else OUT

6.3.4 12 - Interrupt Mask (Reset Value = 0xE0)

This register holds the interrupt enable bits and other configuration information.

CEB[7] – century enable. When 1, the CB bit will toggle when the Year's register rolls over from 999 to 00. When 0, the CB bit will never be automatically updated.

IM[6:5] – interrupt mode. This controls the length of nAIRQ as shown. The interrupt output always goes high when the corresponding flag in the Status Register is cleared. In order to minimize current drawn by the RTC this field should be kept at 0x3.

BLIE[4] – Battery Low interrupt enable. When 1,the Battery Low detection will generate an interrupt.

TIE[3] – Timer interrupt enable. When 1, the Countdown Timer will generate an IRQ signal and set the TIM flag when the timer reaches 0.

AIE[2] – Alarm interrupt enable. When 1, a match of all the enabled alarm registers will generate an IRQ signal.

EX2E[1] – when 1, the WDI input pin will generate the XT2 interrupt when the edge specified by EX2P occurs.

EX1E[0] – when 1, the EXTI input pin will generate the XT1 interrupt when the edge specified by EX1P occurs.

IM Value	Interrupt Pulse Width	
	32 kHz Oscillator	128 Hz Oscillator
00	Level	Level
01	1/8192 s	1/64 s
10	1/64 s	1/64 s
11	1/4 s	1/4 s

6.3.5 12 - SQW (Reset Value = 0x06)

This register holds the control signals for the square wave output. Note that some frequency selections are not valid if the 128 Hz RC Oscillator is selected.

SQWE[7] – when 1, the square wave output is enabled. When 0, the square wave output is held at the value of OUT.

SQFS[4:0] – selects the frequency of the square wave output as shown. Note that some selections are not valid if the 128 Hz oscillator is selected. Some selections also produce short pulses rather than square waves, and are intended primarily for test usage.

Square Wave Function Select	
SQFS Value	**Square Wave Output**
00000	1 century (**)
00001	32 kHz (*)
00010	8 kHz (*)
00011	4 kHz (*)
00100	2 kHz (*)
00101	1 kHz (*)
00110	512 Hz (*) - Default value
00111	256 Hz (*)
01000	128 Hz
01001	64 Hz
01010	32 Hz
01011	16 Hz
01100	8 Hz
01101	4 Hz
01110	2 Hz
01111	1Hz
10000	1/2 Hz
10001	1/4 Hz
10010	1/8 Hz
10011	1/16 Hz
10100	1/32 Hz
10101	1/60 Hz (1 minute)
10110	16 kHz (*)
10111	100 Hz (*) (**)
11000	1 hour (**)
11001	1 day (**)
11010	TIRQ
11011	NOT TIRQ
11100	1 year (**)
11101	1 Hz to Counters (**)
11110	1/32 Hz from Acal (**)
11111	1/8K Hz from Acal (**)

(*) - NA if 128 Hz Oscillator selected
(**) - Pulses for Test Usage

6.4 Calibration Registers

6.4.1 14 - Calibration XT (Reset Value = Preconfigured)

This register holds the control signals for a digital calibration function of the XT Oscillator

CMDX[7] – the calibration adjust mode. When 0 (Normal Mode), each adjustment step is +/- 2ppm. When 1 (Coarse Mode), each adjustment step is =/- 4ppm.

OFFSETX[6:0] – the amount to adjust the effective time. This is a two's complement number with a range of -64 to +63 adjustment steps

6.4.2 15 - Calibration RC Upper (Reset Value = Preconfigured)

This register holds the control signals for the fine digital calibration function of the low power RC Oscillator

CMDR[7:6] – the calibration adjust mode for the RC calibration adjustment. CMDR selects the highest frequency used in the RC Calibration process as shown.

OFFSETRU[5:0] – the upper 6 bits of the OFFSETR field, which is used to set the amount to adjust the effective time. OFFSETR is a two's complement number with a range of -2 ^ 13 to +2 ^ 13 -1 adjustment steps

CMDR	Calibration Period	Minimum Adjustment	Maximun Adjustment
00	8,192 seconds	+/- 1.91 ppm	+/- 1.56%
01	4,096 seconds	+/- 3.82 ppm	+/- 3.13%
10	2,048 seconds	+/- 7.64 ppm	+/- 6.25%
11	1,024 seconds	+/- 15.28 ppm	+/- 12.5%

6.4.3 16 - Calibration RC Lower (Reset Value = Preconfigured)

This register holds the lower 8 bits of the OFFSETR field for the digital calibration function of the low power RC Oscillator.

OFFSETRL[7:0] – the lower 8 bits of OFFSETR

6.5 Sleep Control Resisters

6.5.1 17 - Sleep Control (Reset Value = 0x00)

This register controls the Sleep function of the Power Control system

SLP[7] – when 1, the Power Control SM will transition to the SWAIT state. This bit will be cleared when the SM returns to the RUN state. If either Stop is 1 or no interrupt is enabled, SLP will remain at 0 even after an attempt to set it to 1.

SLRES[6] – when 1, assert nRST low when the Power Control SM is in the Sleep state.

EX2P[5] – when 1, the external interrupt XT2 will trigger on a rising edge of the WDI pin. When 0, the external interrupt XT2 will trigger on a falling edge of the WDI pin.

EX1P[4] – when 1, the external interrupt XT1 will trigger on a rising edge of the EXTI pin. When 0, the external interrupt XT1 will trigger on a falling edge of the EXTI pin.

SLST[3] – set when the RTC enters Sleep Mode. This allows software to determine if a SLEEP has occurred since the last time this bit was read.

SLTO[2:0] – the number of 7.8 ms periods after SLP is set until the Power Control SM goes into the SLEEP state. If SLTO is not 0, the actual delay is guaranteed to be between SLTO and (SLTO + 1) periods. If SLTO is 0, the transition will occur with no delay.

6.6 Timer Resisters

6.6.1 18 - Countdown Timer Control (Reset Value = 0x23)

This register controls the Countdown Timer function. Note that the 00 frequency selection is slightly different depending on whether the 32 kHz XT Oscillator or the 128 Hz RC Oscillator is selected.

TE[7] – Timer Enable. When 1, the Countdown Timer will count down. When 0, the Countdown Timer retains the current value. If TE is 0, the clock to the Timer is disabled for power minimization.

TM[6] – Timer Interrupt Mode. Along with TRPT, this controls the Timer Interrupt function as shown. A Level Interrupt will cause the nIRQ signal to be driven low by a Countdown Timer interrupt until the associated flag is cleared. A Pulse interrupt will cause the nIRQ signal to be driven low for the time shown or until the flag is cleared.

TRPT[5] – Along with TM, this controls the repeat function of the Countdown Timer. If Repeat is selected, the Countdown Timer reloads the value from the Timer Initial register upon reaching 0, and continues counting. If Single is selected, the Countdown Timer will halt when it reaches zero. This allows the generation of periodic interrupts of virtually any frequency.

RPT[4:2] – These bits enable the Alarm Interrupt repeat function, as shown. HA is the Hundredths_Alarm register value.

TFS[1:0] – Select the clock frequency and interrupt pulse width of the Countdown Timer, as defined. RCPLS is a 80 – 120 us pulse.

	Repeat Function	
RPT	**HA**	**Repeat When**
7	FF	Once per hundredth (*)
7	F[9-0]	Once per tenth (*)
7	[9-0][9-0]	Hundredths match (once per second)
6		Hundredths and seconds match (once per minute)
5		Hundredths, seconds, and minutes match (once per hour)
4		Hundredths, seconds, minutes and hours match (once per day)
3		Hundredths, seconds, minutes, hours and weekday match (once per week)
2		Hundredths, seconds, minutes, hours and date match (once per month)
1		Hundredths, seconds, minutes, hours, date and month match (once per year)
0		Alarm Disabled

(*) - Once per second if 128 Hz Oscillator selected

Countdown Timer Function Select

TM	TRPT	TFS	INT	Repeat	Countdown Timer Frequency		Interrupt Pulse Width	
					32 kHz Oscillator	128 Hz Oscillator	32 kHz Oscillator	128 Hz Oscillator
0	0	00	Pulse	Single	4 kHz	128 Hz	1/4096 s	1/128 s
0	0	01	Pulse	Single	64 Hz	64 Hz	1/128 s	1/128 s
0	0	10	Pulse	Single	1 Hz	1 Hz	1/64 s	1/64 s
0	0	11	Pulse	Single	1/60 Hz	1/60 Hz	1/64 s	1/64 s
0	1	00	Pulse	Repeat	4 kHz	128 Hz	1/4096 s	1/128 s
0	1	01	Pulse	Repeat	64 Hz	64 Hz	1/128 s	1/128 s
0	1	10	Pulse	Repeat	1 Hz	1 Hz	1/64 s	1/64 s
0	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/64 s	1/64 s
1	0	00	Level	Single	4 kHz	128 Hz	N/A	N/A
1	0	01	Level	Single	64 Hz	64 Hz	N/A	N/A
1	0	10	Level	Single	1 Hz	1 Hz	N/A	N/A
1	0	11	Level	Single	1/60 Hz	1/60 Hz	N/A	N/A
1	1	00	Pulse	Repeat	4 kHz	128 Hz	1/4096 s	RCPLS
1	1	01	Pulse	Repeat	64 Hz	64 Hz	1/4096 s	RCPLS
1	1	10	Pulse	Repeat	1 Hz	1 Hz	1/4096 s	RCPLS
1	1	11	Pulse	Repeat	1/60 Hz	1/60 Hz	1/4096 s	RCPLS

6.6.2 19 - Countdown Timer (Reset Value = 0x00)

This register holds the current value of the Countdown Timer. I may be loaded with the desired starting value when the Countdown Timer is stopped.

6.6.3 1A - Timer Initial Value (Reset Value = 0x00)

This register holds the value which will be reloaded into the Countdown Timer when it reaches zero if the TRPT bit is a 1. This allows for periodic timer interrups, and a period of (Timer_initial +1) * (1/Countdown_frequency).

6.6.4 1B - Watchdog Timer (Reset Value = 0x00)

This register controls the Watchdog Timer function.

WDS[7] – Watchdog Steering. When 0, the Watchdog Timer will generate WIRQ when it times out. When 1, the Watchdog Timer will generate a reset when it times out.

BMB[6:2] – the number of clock cycles which must occur before the Watchdog Timer times out. A value of 00000 disables the Watchdog Timer function.

WRB[1:0] – the clock frequency of the Watchdog Timer, as shown.

Watchdog Timer Frequency Select	
WRB Value	**Watchdog Timer Frequency**
00	16 Hz
01	4 Hz
10	1 Hz
11	1/4 Hz

6.7 Oscillator Resisters

6.7.1 1C - Oscillator Control (Reset Value = 0x00)

This register controls the overall Oscillator function. It may only be written if the Configuration Key register contains the value 0xA1. An auto calibration cycle is initiated immediately whenever this register is written with a value in the ACAL field which is not zero.

OSEL[7] – When 1, request the RC Oscillator to generate a 128 Hz clock for the timer circuits. When 0, request the XT Oscillator to generate a 32 kHz clock to the timer circuit. Note that if the XT Oscillator is not operating, the oscillator switch will not occur. The OMODE field in the Oscillator Status register indicates the actual oscillator which is selected.

ACAL[6:5] – Controls the automatic calibration function, as described.

AOS[4] – When 1, the oscillator will automatically switch to RC oscillator mode when the system is powered from the battery. When 0, no automatic switching occurs.

FOS[3] – When 1, the oscillator will automatically switch to RC oscillator mode when an oscillator failure is detected. When 0, no automatic switching occurs.

PWGT[2] – When 1, the I/O interface will be disabled when the power switch is active and disabled (PWR2 is a 1 and the OUT2 output is a 1).

OFIE[1] – Oscillator Fail interrupt enable. When 1, an Oscillator Failure will generate an IRQ signal.

ACIE[0] – When 1, an Auto calibration Failure will generate an interrupt.

6.7.2 1D - Oscillator Status Register (Reset Value = 0x00)

This register holds several miscellaneous bits used to control and observe the Oscillators.

XTCAL[7:6] – Extended Crystal Calibration. This field defines a value by which the Crystal Oscillator is adjusted to compensate for low capacitance crystals, independent of the normal Crystal Calibration function controlled by the Calibration XT Register. The frequency generated by the Crystal Oscillator is slowed by 122 ppm times the value in the XTCAL field (0, -122, -244 or -366 ppm).

LKO2[5] – Lock OUT2. If this bit is a 1, the OUTB register bit cannot be set to 1. This is typically used when OUT2 is configured as a power switch, and setting OUTB to a 1 would turn off the switch.

OMODE[4] (read only) – Oscillator Mode. This bit is a 1 if the RC Oscillator is selected to drive the internal clocks, and a 0 if the Crystal Oscillator is selected.

XTF[3] (read only) – Crystal Oscillator Not Operable. This bit is a 1 if the crystal oscillator is not switching, either because a failure has occurred to stop the oscillator or because it is disabled, for example if the RTC is currently operating from the RC oscillator.

OF[1] – Oscillator Failure. This bit is set on a power reset, when both the system and battery voltages have dropped below acceptable levels, It is also set if an Oscillator Failure occurs, indicating that the crystal oscillator is running at less than 8 kHz.

ACF[0] – Set when Autocalibration Failure occurs, indicating that either the RC Oscillator frequency is too different from 128 Hz to be correctly calibrated or the XT Oscillator did not start.

6.8 Miscellaneous Registers

6.8.1 1F - Configuration Key (Reset Value = 0x00)

This register contains the Configuration Key, which must be written with specific values in order to access some registers and functions. The Configuration Key is reset to 0x00 on any register write.

1) Writing a value of 0xA1 enables write access to the Oscillator Control register
2) Writing a value of 0x3C does not update the Configuration Key register, but generates a Software Reset.
3) Writing a value of 0x9D enables write access to the Trickle Register (0x20), the VREF Register (0x21 and the Output Control Register (0x30)

6.9 Analog Control Registers

6.9.1 20 - Trickle (Reset Value = 0x00)

This register controls the Trickle Charger. The Key Register must be written with the value 0x9D in order to enable access to this register.

TCS[7:4] - value of 1010 enables the trickle charge function. All other values disable the Trickle Charger.

Diode[3:2] – Diode Select. A value of 10 inserts a diode into the trickle charge circuit. A value of 01 does not insert a diode. Other values disable the Trickle Charger.

ROUT[3:2] – Output Resistor. This selects the output resistor of the trickle charge circuit, as shown.

Trickle Charge Output Register	
ROUT Value	**Series Register**
00	**Disable**
01	**3 KΩ**
10	**6 KΩ**
11	**11 KΩ**

6.9.2 21 - BREF Control (Reset Value = 0x00)

This register controls the reference voltages used in the Wakeup Control system. The Key Register must be written with the value 0x9D in order to enable access to this register.

BREF[7:4] - this selects the voltage reference which is compared to the battery voltage VBAT to produce the BBOD signal, as shown. The voltage sensing circuitry includes hysteresis to insure that the system does not toggle between VBAT and VCC, and both rising and falling voltages are specified. If the VBAT voltage is above the rising voltage which corresponds to the current BREF setting, BBOD will be set. At that point the VBAT voltage must fall below the falling voltage in order to clear the BBOD bit, set the BAT flag and generate a falling edge BL interrupt. If BBOD is clear, the VBAT voltage must rise above the rising voltage in order to clear the BBOD bit and generate a rising edge BL interrupt.

VBAT Reference Voltage		
BREF Value	**VBAT Falling Voltage (Nom)**	**VBAT Rising Voltage (Nom)**
0000	1.2V	1.35V
0001	1.35V	1.5V
0010	1.5V	1.65V
0011	1.65V	1.8V
0100	1.8V	1.95V
0101	1.95V	2.1V
0110	2.1V	2.25V
0111	2.25V	2.4V
1000	2.4V	2.55V
1001	2.55V	2.7V
1010	2.7V	2.85V
1011	2.85V	3.0V
1100	3.0V	3.15V
1101	3.15V	3.3V
1110	3.3V	3.45V
1111	3.45V	3.7V

This register controls the Crystal Oscillator function. It may only be written if the Configuration Key register contains the value 0x9D. Note that bits 4:0 are initialized with the inverse of the NVMB value.

VREFLV[7:6] – The lower 2 bits of the 4 bit VREFV field which holds the voltage calibration value for the Voltage Reference Oscillator.

VREFT[5:0] – The temperature calibration value for the Voltage Reference Generator

6.9.3 27 - Batmode IO Register (Reset Value = 0x00)

This register holds the IOBM bit which controls the enabling and disabling of the I/O interface when a Brownout Detection occurs. It may only be written if the Configuration Key register contains the value 0x9D. all undefined bits must be written with 0.

IOBM[7] – If 1, the RTC will not disable the I/O interface even if VCC goes away and VBAT is still present. This allows external access while the RTC is powered by VBAT.

6.9.4 2F - Analog Status Register (Read Only)

This register holds eight status bits which indicate the voltage levels of the VCC and VBAT power inputs.

BBOD[7] – if 1, the VBAT input voltage is above the BREF threshold.

BMIN[6] – if 1, the VBAT input voltage is above the minimum operating voltage (1.2 V)

VINIT[1] – if 1, the VCC input voltage is above the minimum power up voltage (1.6 V)

6.9.5 30 - Output Control Register

This register holds bits which control the behavior of the I/O pins under various power down conditions. The Key Register must be written with the value 0x9D in order to enable access to this register.

WDBM[7] – if 1, the WDI input is enabled when the RTC is powered from VBAT. If 0, the WDI input is disabled when the RTC is powered from VBAT.

EXBM[6] – if 1, the EXTI input is enabled when the RTC is powered from VBAT. If 0, the EXTI input is disabled when the RTC is powered from VBAT.

WDDS[5] – if 1, the WDI input is disabled when the RTC is in Sleep Mode. If 0, the WDI input is enabled when the RTC is in Sleep Mode. If WDI is disabled, it will appear as a 1 to the internal logic.

EXDS[4] – if 1, the EXTI input is disabled when the RTC is in Sleep Mode. If 0, the EXTI input is enabled when the RTC is in Sleep Mode. If EXTI is disabled, it will appear as a 1 to the internal logic

RSEN[3] – if 1, the nRST output is enabled when the RTC is in Sleep Mode. If 0, the nRST output is completely disconnected when the RTC is in Sleep Mode.

O4EN[2] – if 1, the CLKOUT/nIRQ3 output is enabled when the RTC is in Sleep Mode. If 0, the CLKOUT/nIRQ3 output is completely disconnected when the RTC is in Sleep Mode.

O3EN[1] – if 1, the nTIRQ output is enabled when the RTC is in Sleep Mode. If 0, the nTIRQ output is completely disconnected when the RTC is in Sleep Mode.

O1EN[0] – if 1, the FOUT/nIRQ output is enabled when the RTC is in Sleep Mode. If 0, the FOUT/nIRQ output is completely disconnected when the RTC is in Sleep Mode.

6.10 Reserved Registers

6.10.1 28 - Reserved

6.10.2 29 - Reserved

6.10.3 2A - Reserved

6.10.4 2B - Reserved

6.10.5 2C - Reserved

6.10.6 2D - Reserved

6.10.7 2E - Reserved

6.11 RAM Registers

6.11.1 3F Extension RAM Address (Reset Value (0x00)

This register controls access to the Extension RAM, and includes some miscellaneous control bits.

O4BM[7] – if 1, the CLKOUT/nIRQ3 output is enabled when the RTC is powered from VBAT. If 0, the CLKOUT/nITQ3 output is completely disconnected when the RTC is powered from VBAT.

BPOL[6] – BL Polarity. When 0, the Battery Low Flag BL is set when the VBAT voltage goes below the BREF threshold. When 1, the Battery Low flag BL is set when the VBAT voltage goes above the BREF threshold.

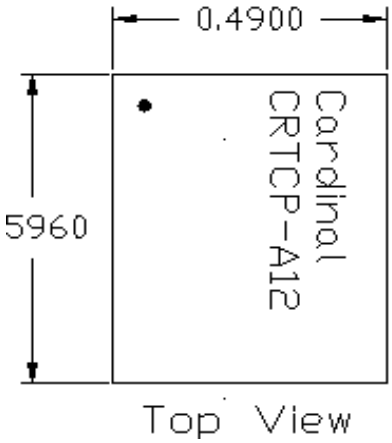
WDIN[5] (read only) – this bit supplies the current level of the WDI pin.

EXIN[4] (read only) – this bit supplies the current level of the EXTI pin.

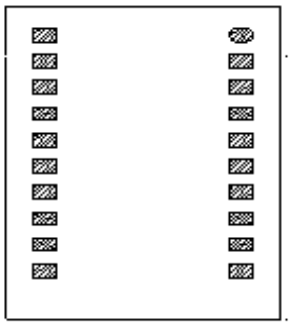
XEN[3] – Extended address enable. When 1, the XADA and XADS fields are used to generate the upper RAM address. When 0, the upper RAM address is forced to zero.

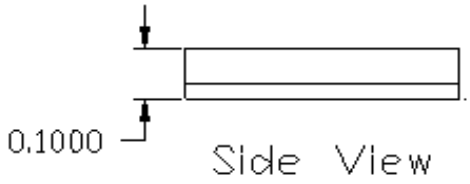
XADA[2] – this field supplies the upper bit for addresses to the Alternate RAM address space.

XADS[1:0] – this field supplies the upper two address bits for the Standard RAM address space.

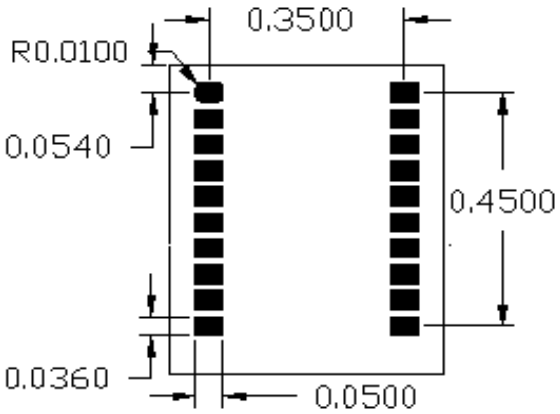


Top View


Bottom View



Side View



Solder Pad Layout

Pin 1 Do not connect.	Pin 20 Vdd
Pin 2 Int.	Pin 19 NC
Pin 3 /Reset	Pin 18 NC
Pin 4 NC	Pin 17 SDA
Pin 5 NC	Pin 16 SCL
Pin 6 NC	Pin 15 Do Not Connect
Pin 7 NC	Pin 14 NC
Pin 8 Enable.	Pin 13 NC
Pin 9 NC	Pin 12 NC
Pin 10 Gnd.	Pin 11 NC