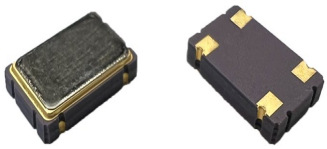
CARDINAL COMPONENTS

CPPD7 Dual Frequency CMOS Clock Oscillator



7.0 x 5.0 x 1.3mm
LCC Ceramic Package

Features

- Factory programmed Dual Frequency (selectable)
- CMOS Output (will interface with TTL devices)
- 3.3V or 5.0V nominal Supply Voltage
- Size: 7 x 5mm

Applications

Driving A/Ds, D/As, FPGAs
Digital Video
Ethernet, GbE
Medical
Storage Area Networking
COTS
Broad Band Access
SONET/ SDH/ DWDM
Test & Measurement

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Condition
Frequency Range	1	-	133	MHz	(3.3V:1 - 100MHz)
Frequency Stability [2]	±25	-	±100	ppm	For all supply voltages, load changes, aging for 1 year at 25°C ± 2°C, shock, vibration and temperatures.
Operating Temperature Range options [2]	0 -20 -40	- - -	+70 +70 +85	°C	
Supply Voltage [1, 2] V_{DD}	2.97	-	5.5	V	See Part Number options on page 2
Supply Current I_{DD} (No Load)	-	-	45 25	mA	V_{DD} = 5.0V V_{DD} = 3.3V
Output Type	CMOS				Cload = 50pF max, V_{DD} = 4.5~5.5V, ≤ 66MHz Cload = 25pF max, V_{DD} = 4.5~5.5V, > 66MHz Cload = 30pF max, V_{DD} = 3.0~3.6V, ≤ 40MHz Cload = 15pF max, V_{DD} = 3.0~3.6V, > 40MHz
	TTL				Cload = 50pF max; V_{DD} = 4.5~5.5V, ≤ 40MHz
Duty Cycle	-	-	-	%	See Page 2
Output V_{OH} (TTL Level)	2.4	-	-	V	V_{DD} = 4.5~5.5V
(CMOS Level)	V_{DD} - 0.4			V	All voltages
Output V_{OL}	-	-	0.4	V	All voltages
Output T_{RISE} and T_{FALL}	-	-	-	ns	See page 2
Startup Time	-	-	2	ms	Time for output to reach specified frequency
RMS Period Jitter	-	40 30	50 40	ps	≤ 33MHz > 33MHz
Period Jitter, Pk-Pk		100 75	250 175	ps	>1,000,000 samples ≤ 33MHz > 33MHz
Storage Temperature Range	-55	-	+125	°C	

Notes:
[1] Place an appropriate power supply bypass capacitor next to device for correct operation
[2] Specified by part number

Duty Cycle

Parameter	Min	Typ	Max	Unit	
TTL @1.4V level; V_{DD} = 4.5~5.5V	45 45 40 40		55 55 60 60	%	Fo ≤ 50 MHz, C_L ≤ 50pF 50 MHz < Fo ≤ 66MHz; C_L ≤ 15pF 66 MHz < Fo ≤ 125MHz, C_L ≤ 25pF 125 MHz < Fo ≤ 133MHz, C_L ≤ 15pF

Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V_{DD} level; V_{DD} = 4.5~5.5V	45 40 40		55 60 60	%	Fo ≤ 66 MHz, C_L ≤ 25pF 66 MHz < Fo ≤ 125MHz; C_L ≤ 25pF 125 MHz < Fo ≤ 133MHz, C_L ≤ 15pF

Parameter	Min	Typ	Max	Unit	
CMOS @ 0.5V_{DD} level; V_{DD} = 3.0~3.6V	45 40		55 60	%	Fo ≤ 40 MHz, C_L ≤ 30pF 40 MHz < Fo ≤ 100MHz; C_L ≤ 15pF

Rise/Fall Time

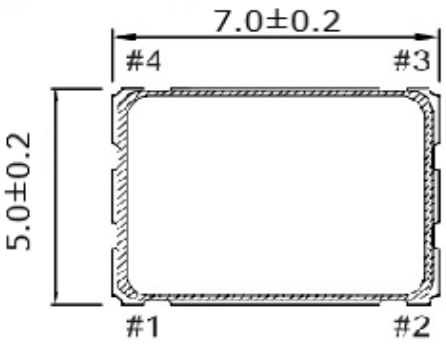
Parameter	Min	Typ	Max	Unit	
Rise/Fall Time			1.8 1.2 0.9 3.4 4.0 2.4	ns	0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=50pF 0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=25pF 0.8V~2.0V, V_{DD} = 4.5~5.5V, C_L=15pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 4.5~5.5V, C_L=50pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 3.0~3.6V, C_L=30pF 0.2V_{DD}~0.8V_{DD}, V_{DD} = 3.0~3.6V, C_L=15pF

Part Number Example: CPPD7LZ-A7BP-50.0/50.125

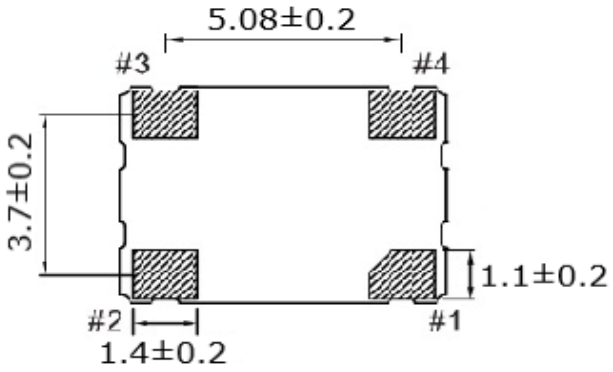
Series Model	Logic	Package Size	Supply Voltage V_{CC}	Packaging	Operating Temperature Range	Frequency Stability (ppm)	Frequency 1 (MHz)	Frequency 2 (MHz)
CPPD	**C**	**7**	**L**	**Z**	**A7**	**BP**	**50.0**	**50.125**
	C=CMOS T = TTL	**7 = 7 x 5mm**	**L = 3.3V** Blank= 5.0V	Blank = Tape Only **Z= Tape/reel**	Blank = 0 to +70°C A5 = -20 to +70°C **A7 = -40 to +85°C**	BR = ±25 **BP = ±50** B6 = ±100	5V: 1 - 133 3.3V: 1 - 100	5V: 1 - 133 3.3V: 1 - 100

Mechanical Dimensions (mm)

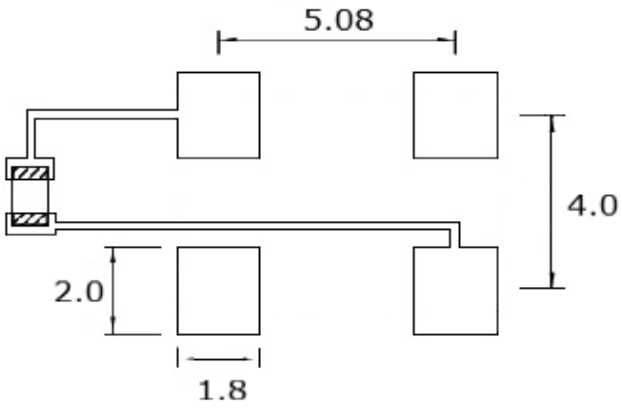
[TOP VIEW]



[BOTTOM VIEW]



[SIDE VIEW]



Pin#	Function
1	Freq Select
2	Gnd
3	Output
4	Vcc

Pin 1 Level	Output
Logic 0	Frequency 1
Logic 1	Frequency 2

Pad Layout
Disclaimer: Recommended layout shown. Adjust layout as needed for individual process requirements.

To ensure optimal oscillator performance, place a by-pass capacitor of 0.01~0.1µF as close to the part as possible between V_{CC} and GND pads.

Contacts (pads): Gold (0.3 to 1.0 µm) over Nickel (1.27 to 8.89 µm)

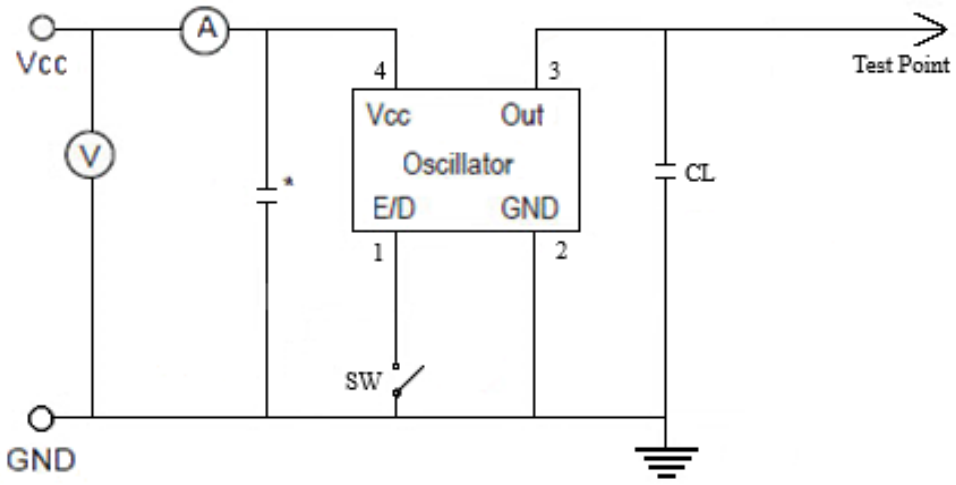
Cardinal Components Inc. certifies this device is in accordance with the RoHS and REACH directives.

Cardinal Components guarantees the device does not contain the following: Cadmium, Hexavalent Chromium, Lead, Mercury, PBB's, PBDE's
Weight of the Device: 0.16 grams
Moisture Sensitivity Level: 1 As defined in J-STD-020D
Second Level Interconnect code: e4

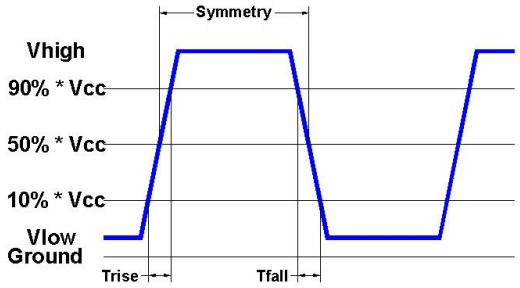
For Optimum Jitter Performance, Cardinal recommends:

- A ground plane under the device
- Do not route large transient signals (both current and voltage) under the device
- Do not place near a large magnetic field such as a high frequency switching power supply
- Do not place near piezoelectric buzzers or mechanical fans

Electrical Test / Load Circuit



Notes:
CL: 15pF Includes the input capacitance of oscilloscope
* 0.01~0.1µF external by-pass filter is recommended



Environmental / ESD Ratings

Reliability: Environmental

Parameter	Condition
Mechanical Shock	MIL-STD-883, Method 2002, Condition B
Vibration	MIL-STD-883, Method 2007, Condition A
Solderability	IPC J-STD-002
Thermal Cycle	MIL-STD-883 Method 1010, Condition B

Thermal Characteristics:
The maximum die or junction temperature is 100°C

ESD Rating

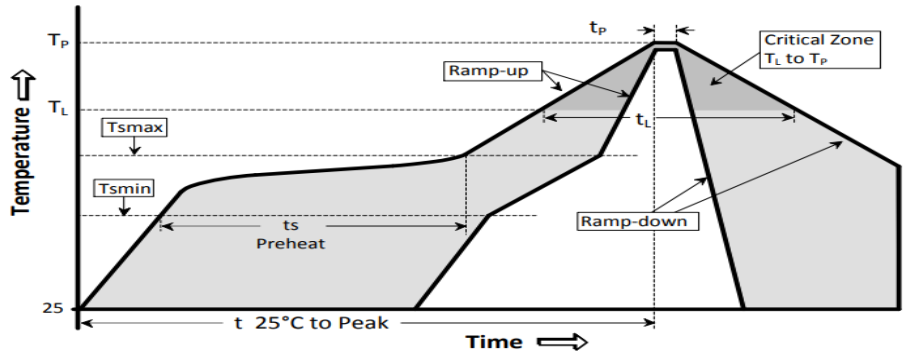
Model	Min. Voltage	Condition
Human Body Model	2000V	MIL-STD-883 3015.7
Machine Model	200V	EIAJ ED-4701/304

Absolute Maximum Ratings

Parameter	Unit
V_{CC} Supply Voltage	-0.5V to +7.0V
Vi Input Voltage	-0.5V to V_{CC} + 0.5V
Vo Output Voltage	-0.5V to V_{CC} + 0.5V

Reflow Cycle

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C "Pb-free"

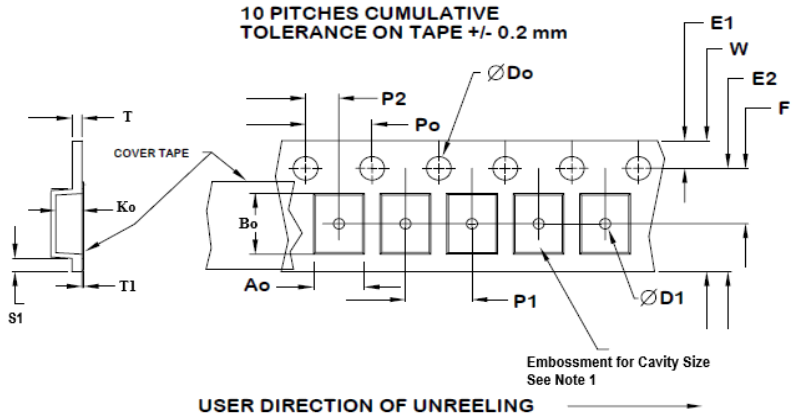


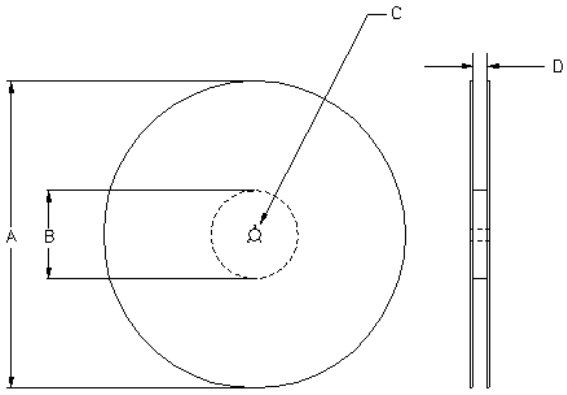
Temperature Profile	Symbol	Condition	Unit
Average ramp-up rate	(Ts_{max} to T_P)	3°C / second max	°C / s
Ramp down Rate	T_{cool}	6°C / second max	°C / s
Time 25°C to Peak Temperature	$T_{to\text{-}peak}$	8 minutes max	min
Preheat			
Temperature min	Ts_{min}	150	°C
Temperature max	Ts_{max}	200	°C
Time Ts_{min} to Ts_{max}	ts	60 – 180	sec
Soldering above liquidus			
Temperature liquidus	T_L	217	°C
Time above liquidus	t_L	60 – 150	sec
Peak temperature			
Peak Temperature	Tp	260	°C
Time within 5°C of peak temperature	tp	20 – 40	sec

The part may be reflowed 2 times without degradation (typical for lead free processing).

Tape and Reel

Tape and Reel available for quantities of 250 to 1000 per reel, cut tape for < 250. 16mm tape, 8mm pitch.





Tape Variable Dimensions Table 2									
Part Size	Tape Size	E2 typ	F	P1	W max	Ao	Bo	Ko	Qty/reel standard
7050	16mm	14.25	7.5 ±0.05	8.0 ±0.1	16.3	5.56±0.1	7.85±0.1	2±0.1	1K

Dimensions in mm Drawings Not to scale
Note 1: Embossed cavity to conform to EIA– 481-B

Tape Constant Dimensions Table 1								
Tape Size	Do	D1 typ	E1	Po	P2	S1 min	T typ	T1 max
16mm	1.5 +0.1 -0.0	1.5	1.75 ±0.1	4.0 ±0.1	2.0 ±0.1	0.6	0.3	0.1

Reel Dimensions (may vary) Table 3						
	A		B		C	D
Reel Size	Inches	mm	Inches	mm	mm	mm
7	7.0	177.8	2.50	63.5	13.0 +0.5 -0.2	Tape size +0.4 +2.0 -0.0
10	10.0	254.0	4.00	101.6		
13	13.0	330.2	3.75	95.3		

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