

### Field Programmable Crystal Oscillator

Series CPPL

- Programmed in the field with the PG-3200 oscillator programming instrument within seconds.
- Factory Programmable
- Can be programmed twice
- Standard Package Options
- Ultra low jitter @ 1 million samples

### Instrument Part Number:

CPPLCL1LZ-A5B6-XX.XXXX TS

CPPL SERIES	C OUTPUT	1 PACKAGE STYLE	L VOLTAGE	Z ADDED FEATURE	A5 OPERATING TEMP	B6 STABILITY	XX.XXXX FREQUENCY	TS TRI-STATE
CPPL	C = CMOS T = TTL	1 = Full Size 4 = Half Size 5 = 3.2x5 Ceramic 7 = 5x7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3V R = 2.7V	Blank = Cut Tape B = Bulk T = Tube Z = Tape and Reel	Blank = 0°C~+70°C A3 = -55~+125°C A5 = -20°C~+70°C A7 = -40°C~+85°C	B6 = ±100PPM BP = ±50PPM BR = ±25PPM	0.500 ~ 133.000MHz	TS = Tri-State PD = Power Down

### Specifications:

Description	Min	Typ	Max	Unit
<b>Frequency Range:</b> Programmable to any discrete frequency	0.500		133	MHz
<b>Available Stability Options:</b>	-100 -50 -25		+100 +50 +25	PPM
<b>Programmable Supply Voltage:</b>				
(1-133 MHz)	4.5	5.0	5.5	V
(1-100 MHz)	3.0	3.3	3.6	V
(1-66.0 MHz)	2.5	2.7	3.0	V
<b>Operating Temperature Range Options:</b>				
	-55		+125	°C
	-20		+70	°C
	-40		+85	°C
<b>Storage Temperature:</b>	-55		+125	°C
<b>Aging:</b> Ta=°25C,Vdd=5V/3.3V			±5	PPM/Year

### Programmable Output Level:

CMOS/TTL

### Operating Conditions:

Description	Min	Max	Unit
<b>V<sub>DD</sub></b> Supply Voltage	2.7	5.5	V
<b>C<sub>TTL</sub></b> Max capacitive load on outputs for TTL levels			
4.5V-5.5V V <sub>DD</sub> , ≤ 40 MHz		50	pF
4.5V-5.5V V <sub>DD</sub> , 40 - 133 MHz		25	pF
<b>C<sub>CMOS</sub></b> Max capacitive load on outputs for CMOS levels			
4.5V-5.5V V <sub>DD</sub> , ≤ 66 MHz		50	pF
4.5V-5.5V V <sub>DD</sub> , 66 - 133 MHz		25	pF
3.0V-3.6V V <sub>DD</sub> , ≤ 40 MHz		30	pF
3.0V-3.6V V <sub>DD</sub> , 40 - 100 MHz		15	pF
2.5-3.0V V <sub>DD</sub> , ≤ 66 MHz		25	pF



**Output Clock Switching Characteristics:**

Description	Test Conditions	Min	Typ	Max	Unit
<b>Duty Cycle:</b> TTL @ 1.4V 4.5-5.5 V <sub>DD</sub>	≤ 50 MHz, C <sub>L</sub> = 50 pF	45	-	55	%
	50 - 66 MHz, C <sub>L</sub> = 15 pF	45	-	55	%
	66 - 125 MHz, C <sub>L</sub> = 25 pF	40	-	60	%
	125 - 133 MHz, C <sub>L</sub> = 15 pF	40	-	60	%
<b>Duty Cycle:</b> CMOS @ V <sub>DD</sub> /2 4.5-5.5 V <sub>DD</sub> 3.0-3.6 V <sub>DD</sub>	≤ 66 MHz, C <sub>L</sub> ≤ 25 pF	45	-	55	%
	66 - 125 MHz, C <sub>L</sub> ≤ 25 pF	40	-	60	%
	125 - 133 MHz, C <sub>L</sub> ≤ 15 pF	60	-	60	%
	≤ 40 MHz, C <sub>L</sub> ≤ 30 pF	45	-	55	%
<b>Rise/Fall:</b>	0.8V - 2.0V, 4.5 - 5.5 V <sub>DD</sub> , C <sub>L</sub> = 50 pF			1.8	ns
	0.8V - 2.0V, 4.5 - 5.5 V <sub>DD</sub> , C <sub>L</sub> = 25 pF			1.2	ns
	0.8V - 2.0V, 4.5 - 5.5 V <sub>DD</sub> , C <sub>L</sub> = 15 pF			0.9	ns
	0.2V - 0.8 * V <sub>DD</sub> , 4.5 - 5.5 V <sub>DD</sub> , C <sub>L</sub> = 50 pF			3.4	ns
	0.2V - 0.8 * V <sub>DD</sub> , 3.0 - 3.6 V <sub>DD</sub> , C <sub>L</sub> = 30 pF			4.0	ns
	0.2V - 0.8 * V <sub>DD</sub> , 3.0 - 3.6 V <sub>DD</sub> , C <sub>L</sub> = 15 pF			2.4	ns
<b>Start Up Time</b>	From Power On	-	-	2	ms
<b>Power Down Delay Time</b> Synchronous Asynchronous	PWR_DOWN pin LOW to output Hi-Z, T = Frequency Oscillator Period		T/2	T+10	ns
			10	15	ns
<b>Output Disable Time</b> Synchronous Asynchronous	OE pin LOW to output Hi-Z, T = Frequency Oscillator Period		T/2	T+10	ns
			10	15	ns
<b>Output Enable Time</b>	T = Frequency Oscillator Period		T	1.5 * T + 25	ns
<b>RMS Period Jitter</b>	1 - 133.00 MHz		8	11	ps
<b>Peak to Peak*</b>	≤ 33.000 MHz		65	99	ps
	> 33.000 MHz		65	80	ps

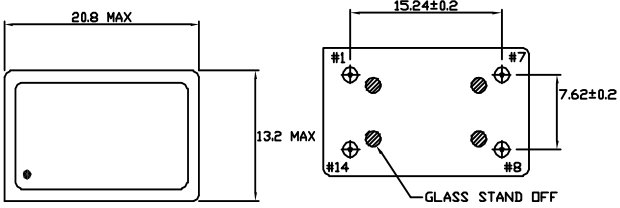
\* Jitter Tested at > 1,000,000 samples, exceeding JEDEC std JESD65

**Electrical Characteristics:**

Description	Test Conditions	Min	Typ	Max	Unit
<b>Input Characteristics (Pin 1):</b>					
V <sub>IL</sub> , Low-Level Input Voltage (To Tri-State or Power Down)	V <sub>DD</sub> = 5.0 V	-	-	0.8	V
	V <sub>DD</sub> = 3.3 V	-	-	0.2 * V <sub>DD</sub>	V
	V <sub>DD</sub> = 2.7 V	-	-	0.2 * V <sub>DD</sub>	V
V <sub>IH</sub> , High-Level Input Voltage (To Enable Output or Open)	V <sub>DD</sub> = 5.0 V	2.0	-	-	V
	V <sub>DD</sub> = 3.3 V	0.7 * V <sub>DD</sub>	-	-	V
I <sub>IL</sub> , Input Low Current	V <sub>IN</sub> = 0 V	-	-	10	μA
I <sub>IH</sub> , Input High Current	V <sub>IN</sub> = V <sub>DD</sub>	-	-	5	μA
<b>Output Characteristics:</b>					
V <sub>OL</sub> , Low-Level Output Voltage	V <sub>DD</sub> = 5.0 V, I <sub>OL</sub> = 16mA	-	-	0.4	V
	V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 8mA	-	-	0.4	V
V <sub>IHTTL</sub> , High-Level Output Voltage	V <sub>DD</sub> = 5.0 V, I <sub>OL</sub> = -16mA	2.4	-	-	V
V <sub>IHCMOS</sub> , High-Level Output Voltage	V <sub>DD</sub> = 5.0 V, I <sub>OL</sub> = -16mA	V <sub>DD</sub> -0.4	-	-	V
	V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = -8mA	V <sub>DD</sub> -0.4	-	-	V
<b>Power Supply Current:</b> (Unloaded)	V <sub>DD</sub> = 5.0 V, F <sub>O</sub> ≤ 133 MHz	-	-	45	mA
	V <sub>DD</sub> = 3.3 V, F <sub>O</sub> ≤ 100 MHz	-	-	25	mA
	V <sub>DD</sub> = 2.7 V, F <sub>O</sub> ≤ 66.0 MHz	-	-	20	mA
<b>Standby Current:</b>		-	10	50	μA
<b>Tri-State Leakage Current</b>	V <sub>DD</sub> = 5.0 V	-	20	-	μA
<b>Output Enable Mode:</b>	Output is Tri-Stated				
<b>Power Down Mode:</b>	Output is Tri-Stated				

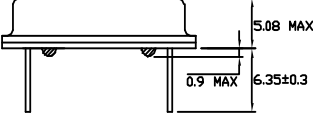
\*Note: Bypass  $V_{DD}$  to GND with a  $0.01\mu\text{F}$  capacitor

#### Style 1 Full Size 14 Pin Dip



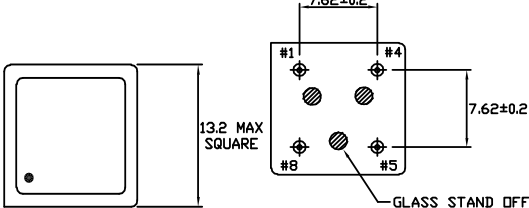
20.8 MAX  
13.2 MAX  
15.24±0.2  
7.62±0.2  
GLASS STAND OFF

Pin #	Function
1	Control
7	GND
8	Output
14	$V_{DD}$



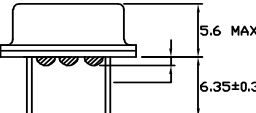
5.08 MAX  
0.9 MAX  
6.35±0.3

#### Style 4 Half Size 8 Pin Dip



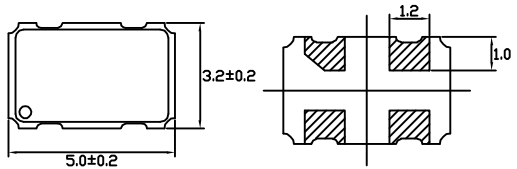
7.62±0.2  
13.2 MAX SQUARE  
7.62±0.2  
GLASS STAND OFF

Pin #	Function
1	Control
4	GND
5	Output
8	$V_{DD}$



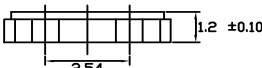
5.6 MAX  
6.35±0.3

#### Style 5 3.2x5 Ceramic SMD

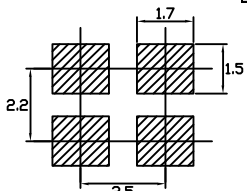


3.2±0.2  
5.0±0.2  
1.2  
1.0

Pin #	Function
1	Control
2	GND
3	Output
4	$V_{DD}$



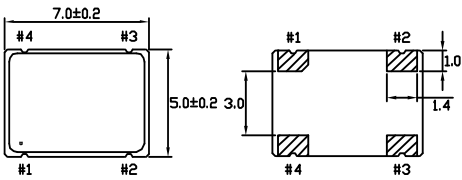
1.2 ±0.10  
2.54



1.7  
1.5  
2.2  
2.5

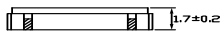
Recommended Solder Pad Layout

#### Style 7 5x7 Ceramic SMD

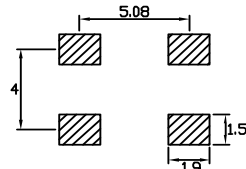


7.0±0.2  
5.0±0.2  
3.0  
1.0  
1.4

Pin #	Function
1	Control
2	GND
3	Output
4	$V_{DD}$



1.7±0.2



5.08  
1.5  
1.9

Recommended Solder Pad Layout

**\*Note: Bypass  $V_{DD}$  to GND with a 0.01 $\mu$ F capacitor**

