

## FASTXO SMD XO Frequency up to 200MHz

Series:CPPY

### Features

- Field Programmable
- CMOS Output (will interface with TTL devices)
- Enable/Disable Function includes low standby power
- Low Jitter
- 1.8V, 2.5V, or 3.3V nominal Supply Voltage
- 1-200 MHz Frequency Range (1-125MHz at 1.8V)
- Fundamental crystals

### Applications

Driving A/Ds, D/As, FPGAs  
 Digital Video  
 Ethernet, GbE  
 Medical  
 Storage Area Networking  
 COTS  
 Broad Band Access  
 SONET/ SDH/ DWDM  
 Test & Measurement



MSL: 1

### Part Numbering Example:

CPPY C 5 L Z A5 B6 xxx.xxxx TS

SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CPPY	C=CMOS	2=2X1.6 Ceramic	L=3.3V	Blank=Blank	Blank=0°C ~ +70°C	B6=±100ppm	1.000~200.000MHz	TS=Tri-State
		3=3.2X2.5 Ceramic	J=2.5V	Z=Tape and Reel	A5=-20°C ~ +70°C	BP=±50ppm		PD=PowerDwn
		5=5X3.2 Ceramic	K=1.8V		A7=-40°C ~ +85°C	BR=±25ppm		
		7=5X7 Ceramic			AJ=-40°C ~ +105°C	BD=±20ppm		
		25=2.5X2.0 Ceramic						

### ELECTRICAL SPECIFICATION

Parameter	3.3V		2.5V		1.8V		Unit	
	Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation	V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V <sub>DD</sub> -10%	V <sub>DD</sub> +10%	V	
Frequency Range	1	200	1	200	1	125	MHz	
Supply Current (@15pf Loading)	-	30	-	28	-	20	mA	
Output Level	Output High	90%V <sub>DD</sub>	-	90%V <sub>DD</sub>	-	90%V <sub>DD</sub>	V	
	Output Low	-	10%V <sub>DD</sub>	-	10%V <sub>DD</sub>	-	10%V <sub>DD</sub>	
Transition Time	Rise Time / Fall Time		-	2	-	2	3	nSec
Duty Cycle	45	55	45	55	45	55	%	
Startup Time	-	5	-	5	-	5	mSec	
Tri-State	Output Enable	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	-	0.7 x V <sub>DD</sub>	V	
	Output Disable	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	-	0.3 x V <sub>DD</sub>	
Stand by Current (@PD Mode)	-	400	-	400	-	400	uA	
Stand by Current (@OE Mode)	-	20	-	20	-	20	mA	
Output Loading	15		15		15		pf	
RMS Phase Jitter (12KHz to 20MHz) @3.3V	-	1	-	1	-	1.5	pSec	
Aging (@ 25°C, First Year)	-	±3	-	±3	-	±3	ppm	
Storage Temp. Range	-50	+125	-50	+125	-50	+125	°C	

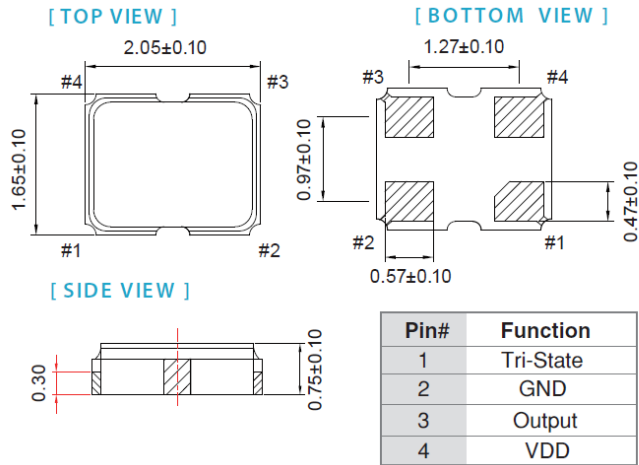
### FREQ. STABILITY vs. TEMP.RANGE

ppm \ °C	±15	±20	±25	±50
-20~+70	O	O	O	O
-40~+85	X	Δ	O	O
-40~+105	X	X	Δ	O

\*O: Available Δ: Conditional X: Not available

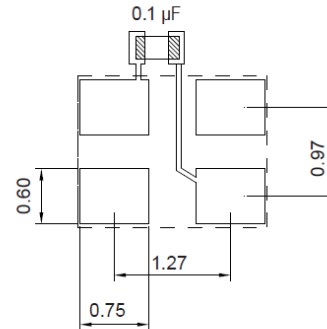
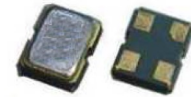
\*Inclusive of calibration @ 25°C, operating temperature range, input Voltage variation, load variation, aging(1st year), shock, and vibration

## Typical 2.05 x 1.65 x 0.75 mm ceramic SMD package

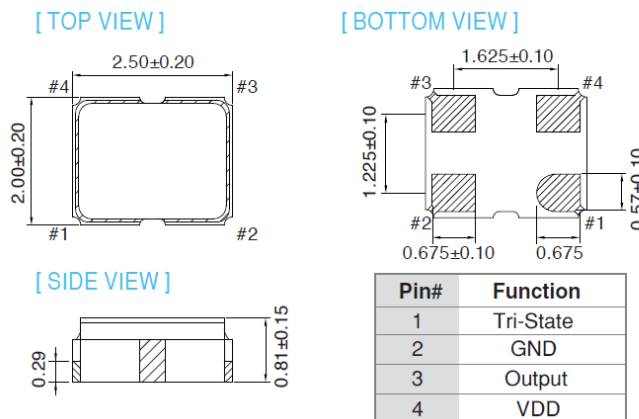


### REQUIRED

To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

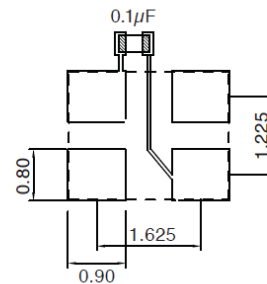
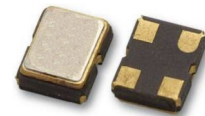


## Typical 2.5 x 2.0 x 0.81 mm ceramic SMD package

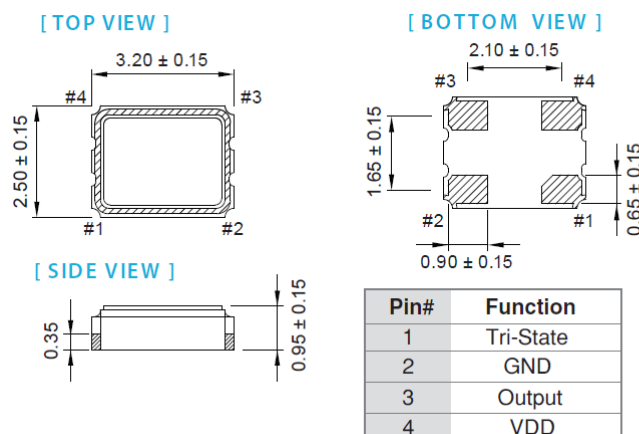


### REQUIRED

To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

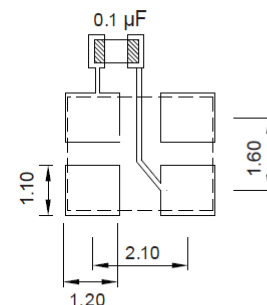
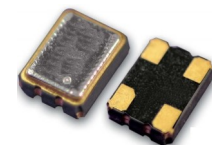


## Typical 3.2 x 2.5 x 0.95 mm ceramic SMD package



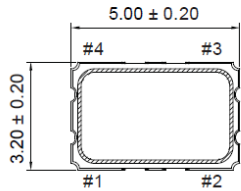
### REQUIRED

To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

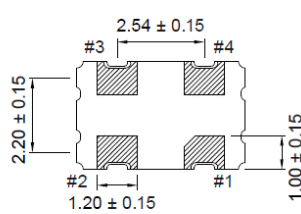


## Typical 5.0 x 3.2 x 1.2 mm ceramic SMD package

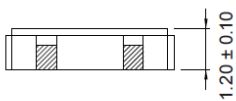
[ TOP VIEW ]



[ BOTTOM VIEW ]



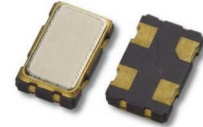
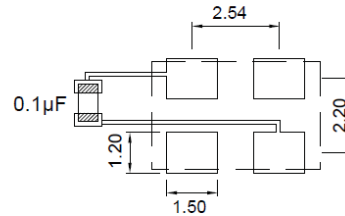
[ SIDE VIEW ]



Pin#	Function
1	Tri-State
2	GND
3	Output
4	VDD

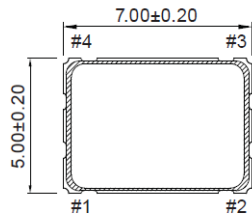
### **REQUIRED**

To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

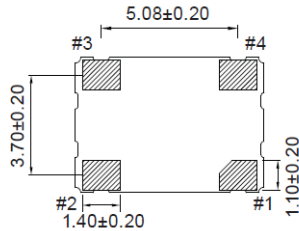


## Typical 7.0 x 5.0 x 1.3 mm ceramic SMD package

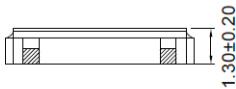
[ TOP VIEW ]



[ BOTTOM VIEW ]



[ SIDE VIEW ]



Pin#	Function
1	Tri-State
2	GND
3	Output
4	VDD

### **REQUIRED**

To ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between Vdd and GND pads.

