FIELD PROGRAMMABLE CRYSTAL OSCILLATOR JITTER

INTRODUCTION

Frequency jitter has become popular in the last few years as a term that defines the short-term stability of a frequency source. A crystal controlled clock oscillator is normally the heart of any digital communication system. Excessive clock jitter can increase the bit error rate (BER) in communication systems. To achieve the best short-term stability in any system, it must start at the oscillator, all other signal processing will only add to the instability. The short-term stability of the system clock usually makes up approximately 10% of the jitter budget.

Frequency instability in a crystal-controlled clock is the unintentional modulation of the generated signal. The unintentional modulation is due to noise generated by the active device in the oscillator stage and buffer stages, crystal noise, and noise conducted into the oscillator by the power source. The crystal clock can oscillate at any frequency within the loaded bandwidth of the oscillator resonator. Although the crystal resonator bandwidth is extremely narrow, the signal generated by the oscillator does have some instability.

Frequency short-term stability is measured and expressed in several different ways. In the frequency domain, single side-band phase noise is specified in dBc/Hz at an offset frequency measured with a spectrum analyzer. In the time domain, Allan Variance is specified as change in output frequency divided by the output frequency over a defined measurement time measured by a frequency counter. In addition, in time domain, frequency jitter is specified in picoseconds measured by an oscilloscope. This paper will describe the frequency jitter measurement technique and test results.

FREQUENCY JITTER MEASURMENTS

Observing the output signal on an oscilloscope, as in figure 1, and measuring the amount of deviation of the signal's period in fractions of a second measure clock jitter. It is defined as the deviation in the output transitions from their ideal position. Measurements can be made in different ways.

Period Jitter: The most popular measurement measures the difference in the period between consecutive non-adjacent clock edges. This paper will show measurements using this method.

Cycle-cycle Jitter: Defined as the deviation in the clock's output period from one cycle to the next.

DESIGN CONSIDERATIONS

The system designer must consider several factors when using clock oscillator in circuits that are sensitive to clock jitter. There are two types of jitter present in the clock signal. One is random jitter and the other is jitter caused by non-random events. The internal random noise and internal modulation cause by spurious internal frequencies generated is the responsibility of the oscillator manufacturer. The random noise and spurious frequencies present on the ground system and power supply bus must be minimized by the system or board level manufacturer. Several essential design features can greatly reduce the chance of introducing noise that will unintentionally modulate the clock oscillator.

- Be sure that there is an adequate single ground plane to prevent ground bounce and spurious oscillations.
- Since a 100 MHz clock with a 1 nanosecond rise and fall time generates odd harmonics frequencies well into the microwave region, excellent RF and Microwave power line bypassing is very important. A minimum of 4.7 uF in parallel with a 0.01 uF is the recommended by-pass on the oscillator input power leads.
- The signal lines from the oscillator to the load must be short and have low inductance. If inductance is present on the signal line, this will cause ringing on the output waveform due to the stray capacitance to ground.
- The power supply bus should be free of system spurious signals, voltage regulator noise, and ripple.
- Be sure the clock is loaded properly and is not reflecting spurious signals back into the clock output. The output waveform must have clean rise and fall edges.

JITTER TESTING SET UP AND METHOD

Several factors must be considered when making jitter measurements.

- Use of a high performance, wide bandwidth oscilloscope with high-speed clock jitter analysis software.
- Maximize the number of measured values (greater than 25,000) for a peak-to-peak measured sigma at or near +/-4.
- Use an oscilloscope sampling rate of 8 GS/Second to capture multiple samples on the leading edge.
- Use a well-designed test fixture with proper clock load to preserve the cleanliness of the signal edges.
- The oscillator under test must use a low noise power source. It is recommended to use a 4.7 uF capacitor in parallel with a 0.01 uF capacitor on the power line next to the oscillator.

JITTER MEASUREMENT BLOCK DIAGRAM

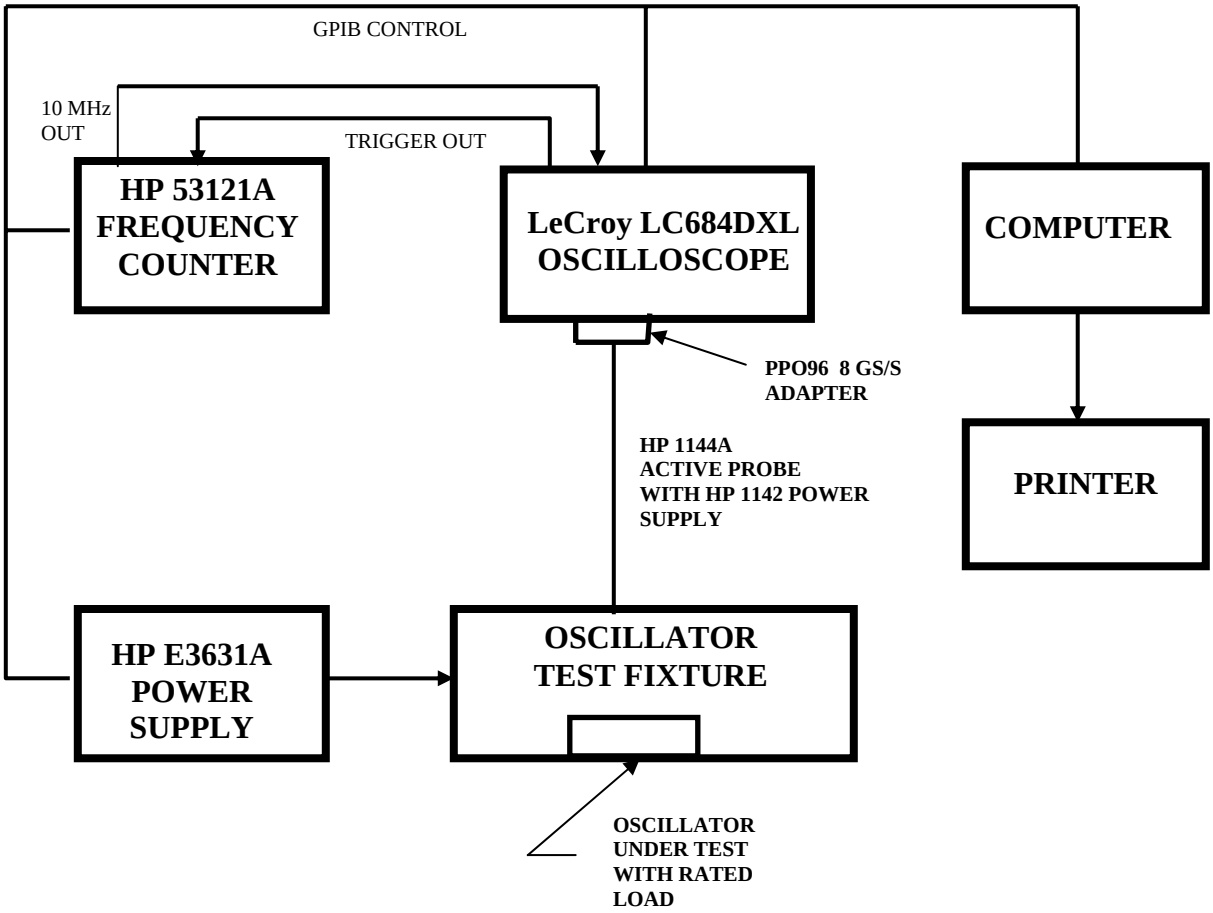

FIGURE 1

JITTER TEST RESULTS OF THE FIELD PROGRAMMABLE OSCILLATORS

The typical oscilloscope screen is shown in Figure 2. This presentation displays the normal gaussian shape distribution showing only random jitter. Under this condition, the value for sigma is the RMS jitter and the range is the peak-to-peak jitter.

TYPICAL OSCILLOSCOPE SCREEN

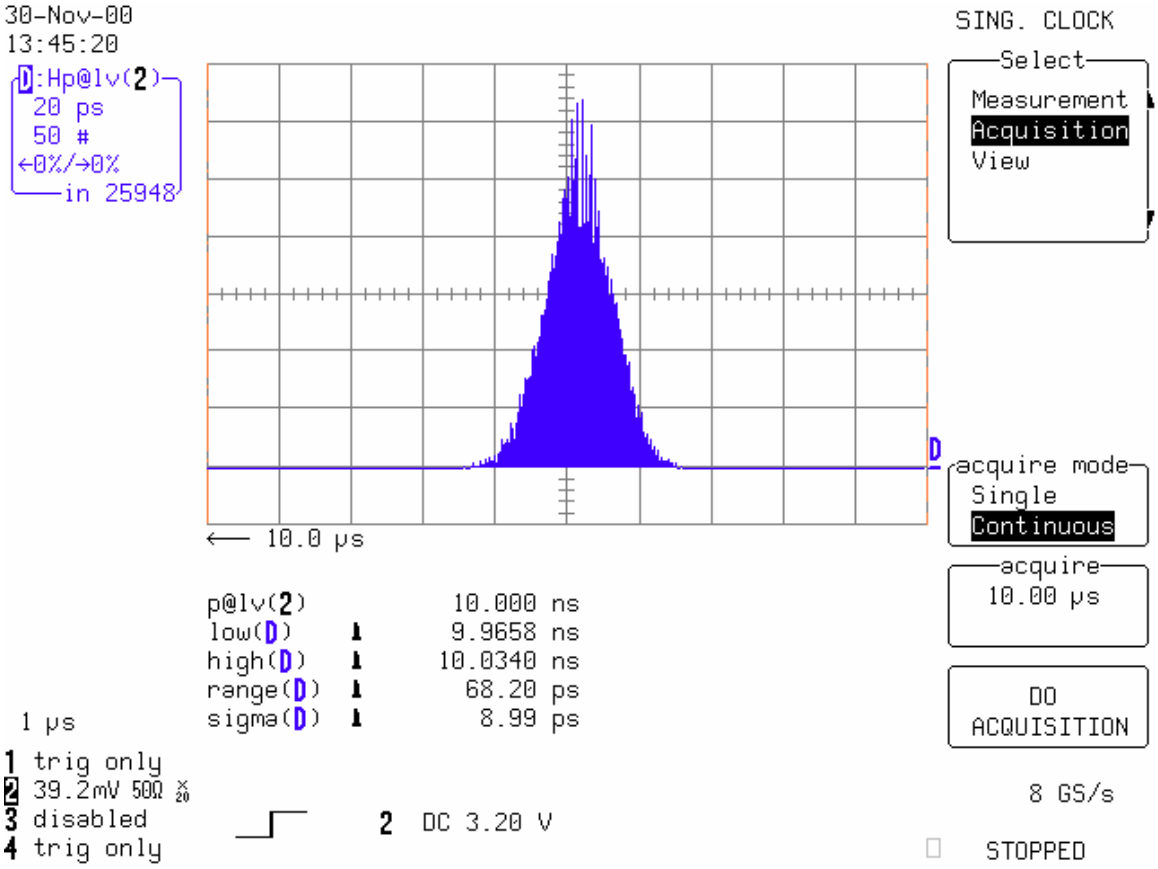

FIGURE 2

Figure 3 shows the RMS jitter and figure 4 shows the peak-to-peak jitter of the Cardinal Components CPPC Series Programmable Oscillator compared to the competition programmable oscillator. The curves represent the aggregate of the data on 176 Cardinal Component's units and 60 of the competition units. The units tested were combination of full size DIP through hole mountable, half size DIP through hole mountable, and 5 x 7 mm surface mountable packages. They are also a mixture of 3.3 volt and 5.0 volt input devices ranging from an output frequency of 3.74 MHz to 155.52 MHz.

RMS JITTER MEASUREMENT RESULTS

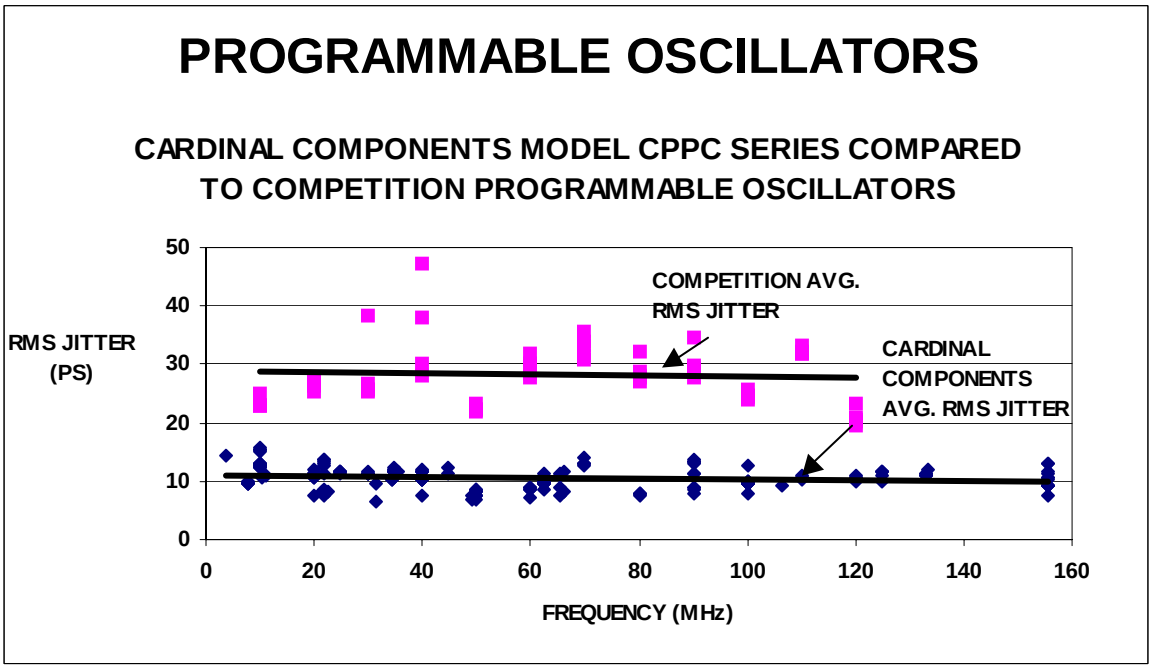

FIGURE 3

PEAK-TO-PEAK JITTER RESULTS

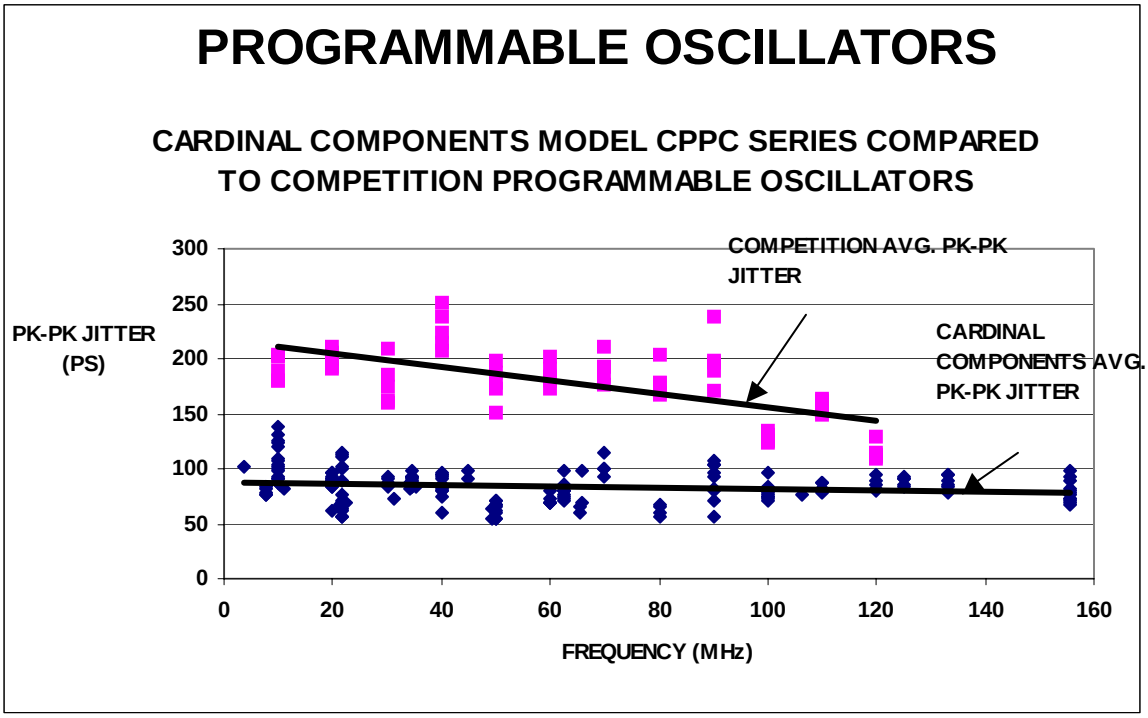

FIGURE 4

Figure 5 shows the RMS jitter and figure 6 shows the peak-to-peak jitter of the Cardinal Component Programmable Oscillator Series compared to the competition **non-programmable** oscillator. The curves represent the aggregate of the data on 176 Cardinal Components Programmable units and 82 **non-programmable** competition units from nine different manufactures. The units tested were combination of full size DIP through hole mountable, half size DIP through hole mountable, and 5 x 7 mm surface mountable packages. The oscillators are a mixture of 3.3 volt and 5.0 volt input devices ranging from an output frequency of 3.74 MHz to 155.52 MHz.

RMS JITTER MEASUREMENT RESULTS

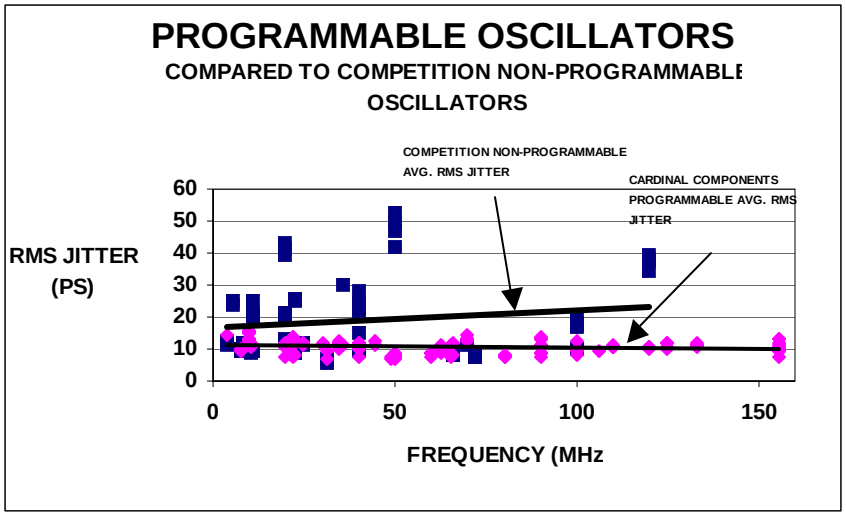

FIGURE 5

PEAK-TO-PEAK JITTER RESULTS

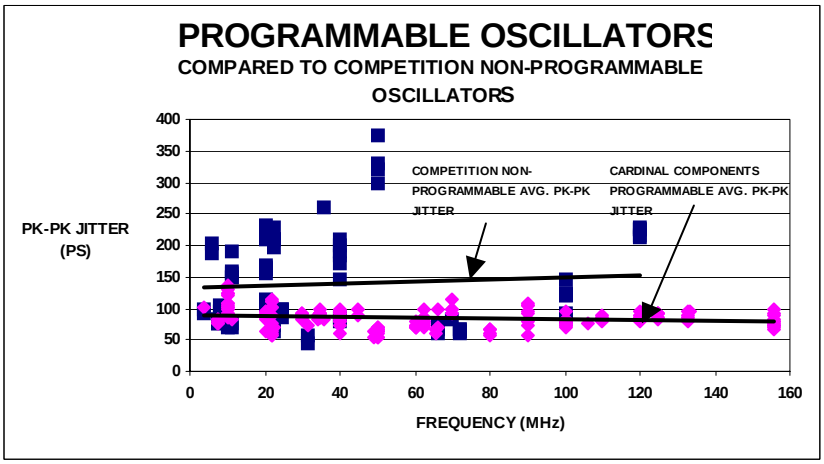

FIGURE 6

CONCLUSION AND SUMMARY

Several different manufacturers have manufactured programmable oscillators over the last few years. They have had a history of poor jitter. Many system designers because of their bad short-term stability have avoided most programmable oscillators. The market, however, desires and need field programmable oscillators. The data presented here clearly shows that not only is the new field-programmable Cardinal Component's oscillator series better than any other that exists; it is also equal to or better than most non programmable units over the frequency range tested.

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