

## Crystal Oscillator

- Factory Programmable
- Standard Package Options
- Also available in 1.8 V

Series **CPW**



Part Numbering Example: CPW C 7 L Z – A7 B6 - XX.XXXX TS

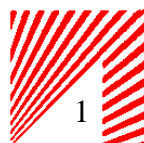
CPW	C	7	L	Z	A7	B6	XX.XXXX	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP	STABILITY	FREQUENCY	TRI-STATE
CPW	C=CMOS	3=3.2x2.5 Ceramic 5=3.2x5 Ceramic 7=5x7 Ceramic	L=3.3V R=2.5V Q=1.8V	Blank=Bulk T=Tube Z=Tape and Reel	A7=-40°C+85°C	B6=±100ppm BP=±50ppm	1.000~166.000 MHz	TS=Tri-State PD=PowrDwn

### Specifications:

Description	Min	Typ	Max	Unit
<b>Frequency Range:</b> Programmable to Any Discrete Frequency	1.0		166.0	MHz
<b>Available Stability Options:</b>	-100		100	ppm
	-50		50	ppm
	-25		25	ppm
<b>Programmable Supply Voltage:</b> (1-166 MHz)	3.0	3.3	3.6	V
(1-166 MHz)	2.2	2.5	2.8	V
(1-166 MHz)	1.6	1.8	2.0	V
<b>Operating Temperature Range:</b>	-40		+85	°C
<b>Storage Temperature:</b>	-55		+125	°C
Aging (PPM/Year) Ta=25C, Vdd=3.3V			±5	

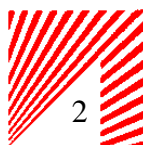
### Operating Conditions:

Description	Min	Max	Unit
Vdd Supply Voltage	1.6	3.6	V
CCMOS Max Capacitive Load on outputs for CMOS levels		15	pF



## ELECTRICAL CHARACTERISTICS

Description	TEST CONDITIONS	Min	Typ	Max	Unit
<b>Input Characteristics (Pin 1):</b> V <sub>IL</sub> , Low-Level Input Voltage TO DISABLE OUTPUT				0.2V <sub>dd</sub>	V
V <sub>IH</sub> , High-Level Input Voltage TO ENABLE OUTPUT or OPEN		0.8V <sub>dd</sub>			V
I <sub>IL</sub> , Input Low Current I <sub>IH</sub> , Input High Current	V <sub>IN</sub> = 0V V <sub>IN</sub> = V <sub>dd</sub>			10 10	μA μA
<b>Output Characteristics:</b> V <sub>OL</sub> , Low-Level Output Voltage	1.8V-2.5V V <sub>dd</sub> , 4mA I <sub>oL</sub> 3.0V-3.6V V <sub>dd</sub> , 8 mA I <sub>oL</sub>			0.1V <sub>dd</sub> 0.4	V
V <sub>OHC</sub> MOS, High-level CMOS Voltage	1.8V-2.5V V <sub>dd</sub> , 4mA I <sub>oL</sub> 3.0V-3.6V V <sub>dd</sub> , -8 mA I <sub>oL</sub>	0.9 V <sub>dd</sub> V <sub>dd</sub> -0.4			V
<b>Power Supply Current: (unloaded)</b>	1 MHz ≤ f <sub>0</sub> ≤ 25 MHz	3.5		4.0	mA
	25 MHz < f <sub>0</sub> ≤ 50 MHz	5.0		6.5	mA
	50 MHz < f <sub>0</sub> ≤ 75 MHz	6.0		8.5	mA
	75 MHz < f <sub>0</sub> ≤ 100 MHz	7.0		10.5	mA
	100 MHz < f <sub>0</sub> ≤ 125 MHz	8.5		12.5	mA
	125 MHz < f <sub>0</sub> ≤ 166 MHz	10.0		15.0	mA
<b>Standby Current:</b>			10	50	uA
<b>Pull-Up (Pin 1)</b>	3.0 – 3.6 V <sub>dd</sub> , V <sub>IN</sub> = 0V 3.0 – 3.6 V <sub>dd</sub> , V <sub>IN</sub> = 0.7V	1.0 50	3.0 100	6.0 200	MΩ KΩ
<b>Tri-State Leakage Current</b>	3.3 V <sub>dd</sub>			50	μA
<b>Output Enable Mode:</b>	Output is Tri-Stated				
<b>Power Down Mode:</b>	Output is Tri-Stated.				



## OUTPUT CLOCK SWITCHING CHARACTERISTICS

Description	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle:		45		55	%
Output Clock Rise/Fall	15pF			1.5	ns
Start Up Time	From power on		5	10	ms
Power Down Delay Time					
Synchronous	PWR_DWN pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous				100	ns
Output Disable Time					
Synchronous	OE pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous	T = Frequency oscillator period			100	ns
Output Enable Time					
Synchronous	OE pin LOW to output Hi-Z			1.5T+100	ns
Asynchronous	T = Frequency oscillator period			100	ns
RMS Period Jitter:	< 33.000 MHz		6		ps
	> 33.000, MHz		7		ps
Peak to Peak *	< 33.000 MHz		80		ps
	> 33.000 MHz		60		ps

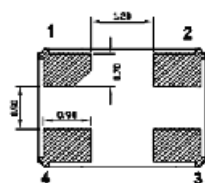
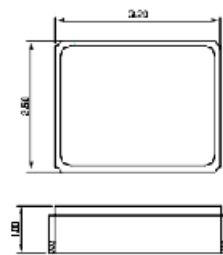
\* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

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Series **CPW**

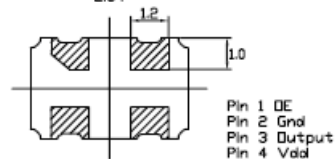
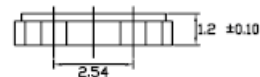
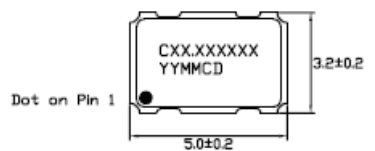
Note: *Bypass Vdd to GND with a 0.01  $\mu$ F capacitor*

## Style 3 3.2x2.5 Ceramic SMD

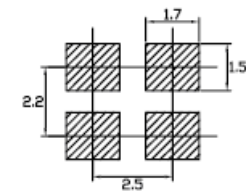


**PIN FUNCTION**  
 1 CONTROL  
 2 GND  
 3 OUTPUT  
 4 Vdd

## Style 5 3.2x5 Ceramic SMD

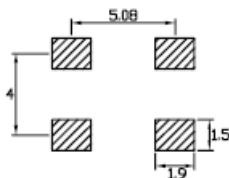
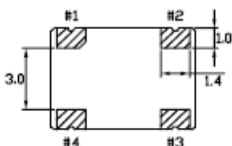
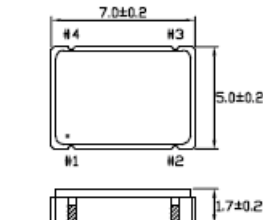


Pin 1 OE  
 Pin 2 Gnd  
 Pin 3 Output  
 Pin 4 Vdd



Recommended solder pad layout

## Style 7 5x7 Ceramic SMD



**PIN FUNCTION**  
 1 CONTROL  
 2 GND  
 3 OUTPUT  
 4 Vdd

