

## Factory Prog. 5 Output PECL TCXO

- Full Custom Multi-Frequency Programmable Osc
- Reduced EMI by turning off unused output
- Factory Programmable
- Differential PECL Output
- Industry-standard packaging saves on board space
- Mult. outputs 1 pkg vs. mult. osc & assoc. comp.
- Performs well under all conditions

## Applications

- High-end multimedia
- Communications
- Industrial
- A/D converters
- Consumer Applications
- Low tolerance applications
- Low-power applications

Series **CCT5E**



Part Numbering Example: **CCT5E 1A 200.0 - 150.0 / 125.0 / 100.0**

<b>CCT5E</b>	<b>1A</b>	<b>200</b>	<b>150</b>	<b>125</b>	<b>100</b>
<b>SERIES</b>	<b>PACKAGE STYLE</b>	<b>FREQUENCY P/P-</b>	<b>FREQUENCY A</b>	<b>FREQUENCY B</b>	<b>FREQUENCY C</b>
	1A=14 pin dip 9=9.6x11.4 SMD	100-400 MHz PECL	0.2 - 200 MHz	0.2 - 200 MHz	0.2 - 200 MHz

Specifications:	Min	Typ	Max	Unit
<b>Frequency Range:</b>				
Output PECL +	100		400	MHz
Output PECL -	100		400	MHz
Output A CMOS	0.2		200	MHz
Output B CMOS	0.2		200	MHz
Output C CMOS	0.2		200	MHz
<b>Available Stability Options:</b>	-2.5		2.5	ppm
<b>Supply Voltage:</b>	3.135	3.3	3.465	V
<b>Operating Temperature Range Options:</b>	-40		85	°C
<b>Storage Temperature:</b>	-55		125	°C
<b>Duty Cycle:</b>	40 45		60 55	% %
<b>Start-Up Time:</b>		3	10	mS
<b>Aging (PPM/1st Year):</b> Ta=25C, Vdd=3.3V			±1	ppm
<b>Static Discharge Voltage</b> Mil-Std 883, method 3015	2000			V
<b>Output Load: *</b> CMOS, < 40 MHz CMOS, ≥ 40 MHz			30 15	pF pF
<b>Output Level:</b>	PECL/CMOS			
<b>Packaging:</b>	25 / Tube Tape & Reel			14 pin SMD

Notes: Recommended .01 µF bypass capacitor from Vcc to GND. Capacitor should be as close to oscillator as possible.  
\* LV PECL outputs require an external termination network



**Electrical Characteristics**

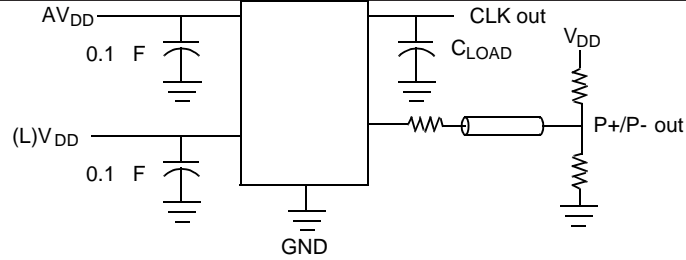
DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
Ioh	Output High Current	Voh = (L)Vdd - 0.5, (L)Vdd = 3.3 V	12	24		mA
Iol	Output Low Current	Vol = .5, (L)Vdd = 3.3 V	12	24		mA
Vih	High Level Input Voltage	CMOS levels, % of Vdd	0.7			V
Vil	Low-Level Input Voltage	CMOS levels, % of Vdd			0.3	V
Iih	Input High Current	Vin = AVdd - 0.3 V		<1	10	µA
Iil	Input Low Current	Vin = + 0.3 V		<1	10	µA
Ioz	Output Leakage Current	tri-state outputs			10	µA
Idd	Total Power Supply Current	Example 1: 1 PECL output @155.52 MHz 1 CMOS output @19.44 MHz 1 CMOS output @38.88 MHz 1 CMOS output @77.76 MHz Example 2: 1 PECL output @400 MHz 1 CMOS output @106.25 MHz 1 CMOS output @200 MHz 1 CMOS output @100 MHz		29		mA
				59		mA
Idds	Shutdown Power Supply Curr	Shutdown active		5	20	µA

**Output Clock Switching Characteristics**

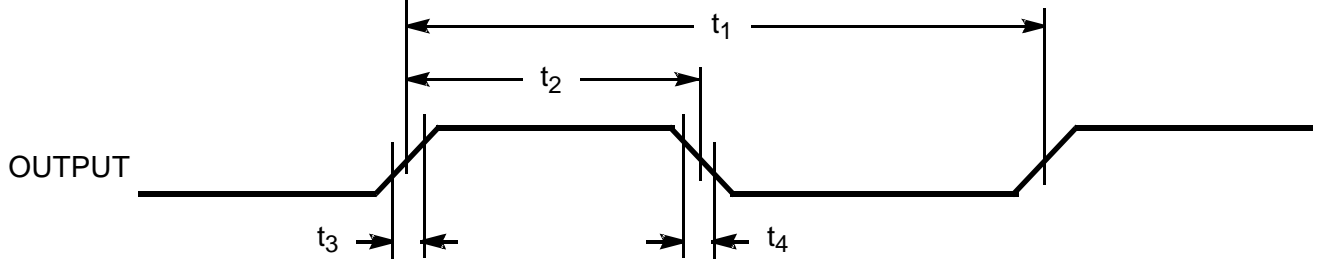
DESCRIPTION		CONDITIONS	MIN	TYP	MAX	UNIT
1/t1	Output Frequency	Clock output limit, CMOS, Commercial	0.2		200	MHz
		Clock output limit, PECL, Commercial	100		400	MHz
t3	Rising Edge Slew Rate	Output clock rise time, 20% – 80% Vdd	0.75	1.4		nS
t4	Falling Edge Slew Rate	Output clock fall time, 20% – 80% Vdd	0.75	1.4		nS
t5	Output tri-state timing after SD/OE switches	Time for output to enter/leave tri-state mode		150	300	nS
t6	Clock Jitter measured at Vdd/2	Peak-to-Peak period jitter, CLK outputs		200		pS
v7	P+/P- Crossing Point	Crossing point ref. to Vdd/2, bal res. net	-0.2	0	0.2	V



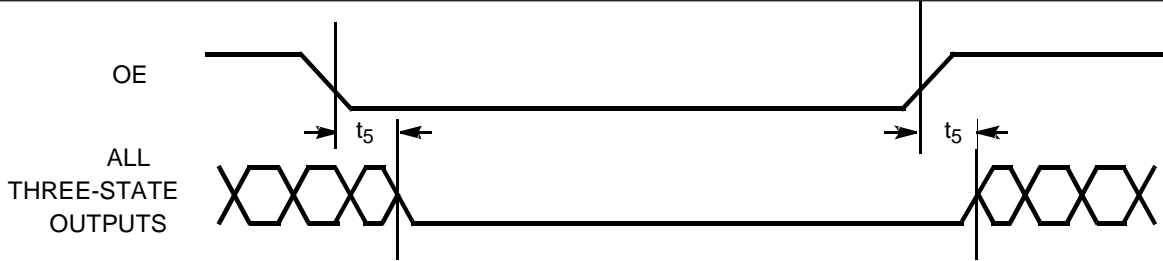
TEST CIRCUIT



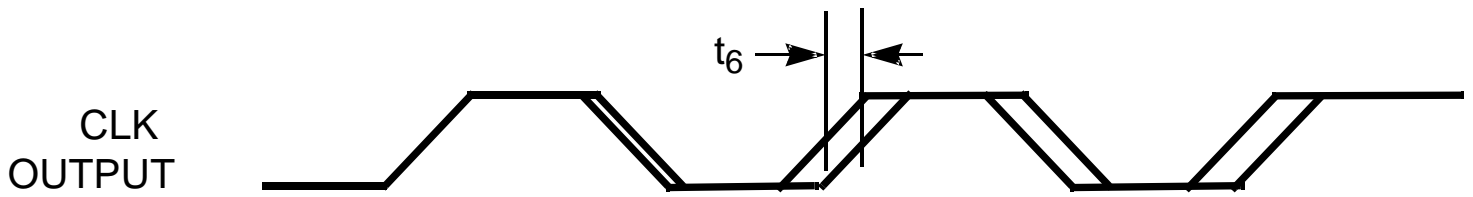
ALL OUTPUTS, DUTY CYCLE, RISE/FALL TIME



OUTPUT 3-STATE TIMING



CLK OUTPUT JITTER



P+/P- CROSSING POINT AND JITTER

