Phase Locked Loop Basics
An Introduction To Phase Locked Loops

Phase Locked Loops (PLL) circuits are used for frequency control. They can be configured as frequency multipliers, demodulators, tracking generators or clock recovery circuits. Each of these applications demands different characteristics but they all use the same basic circuit concept.

Figure 1 contains a block diagram of a basic PLL frequency multiplier. The operation of this circuit is typical of all phase locked loops. It is basically a feedback control system that controls the phase of a voltage controlled oscillator(VCO). The input signal is applied to one input of a phase detector. The other input is connected to the output of a divide by N counter. Normally the frequencies of both signals will be nearly the same. The output of the phase detector is a voltage proportional to the phase difference between the two inputs. This signal is applied to the loop filter. It is the loop filter that determines the dynamic characteristics of the PLL. The filtered signal controls the VCO. Note that the output of the VCO is at a frequency that is N times the input supplied to the frequency reference input.
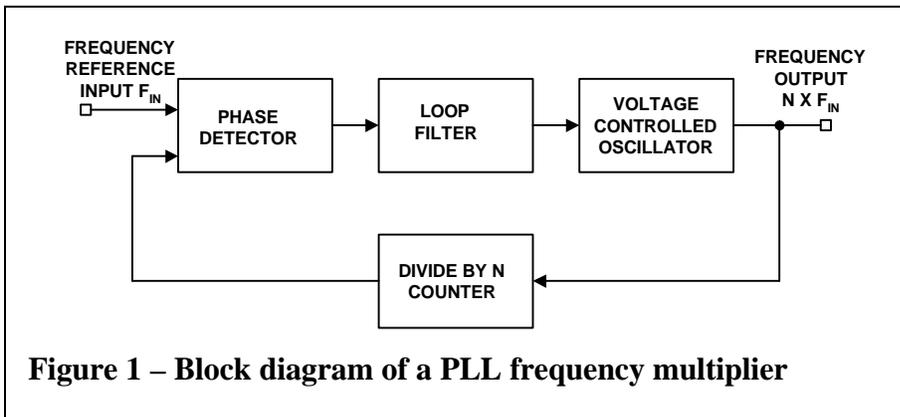

Figure 1 – Block diagram of a PLL frequency multiplier

This output signal is sent back to the phase detector via the divide by N counter.

Normally the loop filter is designed to match the characteristics required by the application of the PLL. If the PLL is to acquire and track a signal the bandwidth of the loop filter will be greater than if it expects a fixed input frequency. The frequency range which the PLL will accept and lock on is called the capture range. Once the PLL is locked and tracking a signal the range of frequencies that the PLL will follow is called the tracking range. Generally the tracking range is larger than the capture range. The loop filter also determines
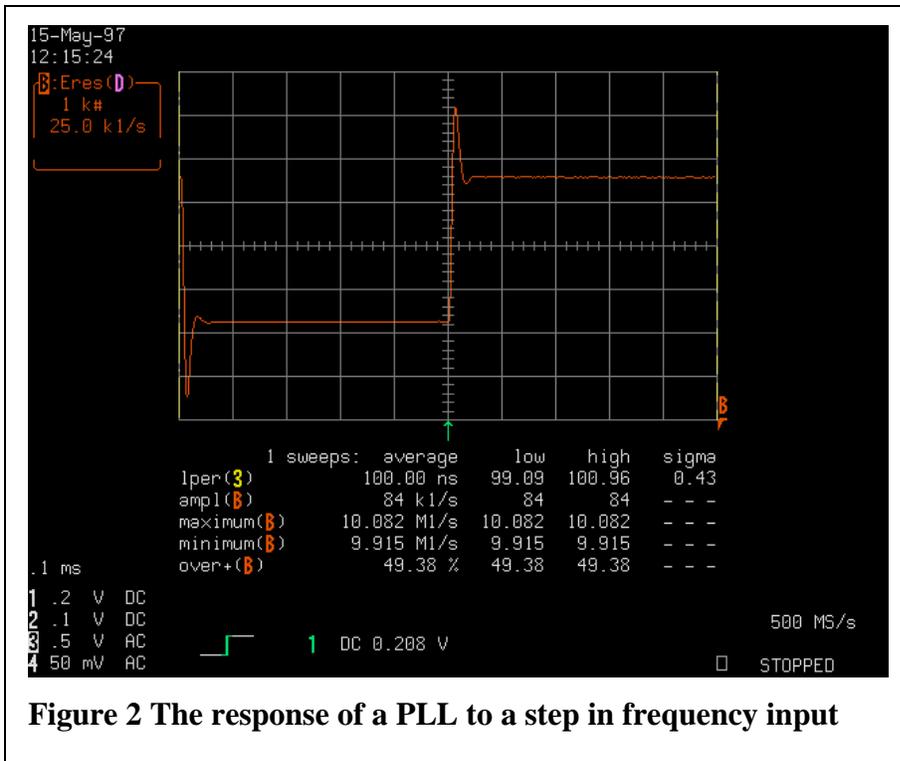

Figure 2 The response of a PLL to a step in frequency input

how fast the signal frequency can change and still maintain lock.   This is the maximum slewing rate.   The narrower the loop filter bandwidth the smaller the achievable phase error.   This comes at the expense of slower response and reduced capture range.

An example of typical measurement of PLL dynamic response is shown in figure 2. This PLL is used in a frequency synthesizer and shows the response to an 80 kHz step in the 10 MHz reference input.   This circuit has a capture range of about +/- 5% of center frequency.

Note that the frequency of the PLL, the vertical axis, shows a 50 % overshoot. This slightly under damped response is a compromise which achieves faster slew rate tolerance and moderate capture range.

There are a variety of ways that a LeCroy oscilloscope can be used in PLL measurements. Modern,   high   performance microprocessors often employ internal PLL's to multiply the system clock frequency.   The manufacturers   specify   the maximum cycle to cycle period variation that is allowed on the system clock.   A typical specifcation   is   that   the maximum jitter be less than 250 ps peak to peak. Since the output of the PLL is not accessible it is important that the system clock input meet this
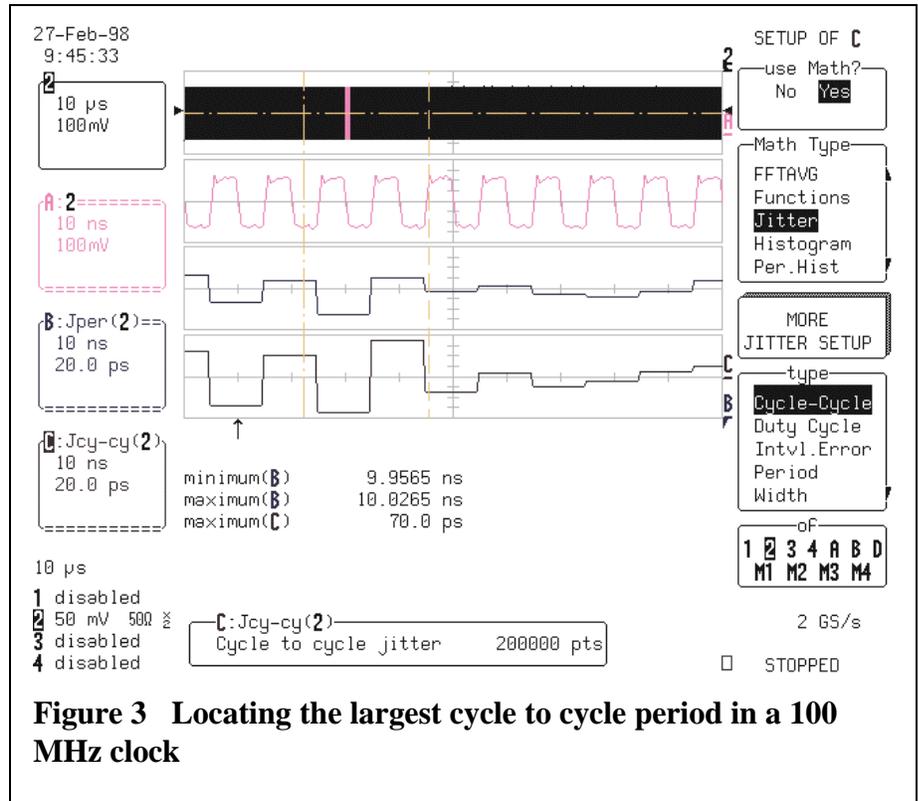

Figure 3   Locating the largest cycle to cycle period in a 100 MHz clock

specification.   Engineers can verify that the system clock meets this specification by measuring the system clock using JitterTrack cycle to cycle. This is illustrated in figure 3. In   a   100   us   record   the maximum cycle to cycle period difference is 70 ps. This value was read directly from the JitterTrack   cycle   to   cycle waveform in trace C. The area between the vertical parameter cursors marks the maximum. Trace A is a zoom expansion of the acquired data and shows the two adjacent cycles which have the   maximum   difference. Trace B is the JitterTrack Period which reads the absolute period of each cycle of the clock waveform.

If the PLL is accessible LeCroy scopes can be used to verify the linearity of the phase detector by plotting the trend of mean output level versus input phase difference.

LeCroy oscilloscopes offer a wide variety of measurement tools for characterizing phase locked loops. Jitter and timing analysis is the primary tool for evaluation of these precision time base circuits.