

Low Noise Oscillator

- *Tight Frequency*
- *High Stability (Low Jitter)*
- *Standard Package Options*

Series **CC155**



Part Numbering Example: CC155 C 1 L Z - A5 B6 - 155.52 TS

CC155	C	1	L	Z	A5	B6	155.52	TS
SERIES	OUTPUT	PACKAGE STYLE	VOLTAGE	ADDED FEATURES	OPERATING TEMP.	STABILITY	FREQUENCY	TRI-STATE
CC155	C = CMOS T = TTL	1 = Full Size 4 = Half Size 7 = 5X7 Ceramic 8 = PLASTIC SMD	Blank = 5V L = 3.3 V	Blank = Bulk T = Tube Z = Tape and Reel	Blank = 0°C +70°C A5 = -20°C +70°C A7 = -40°C +85°C	B6 = ±100 ppm BP = ±50 ppm BR = ±25 ppm	155.52 MHz	TS = Tri-State PD=PowerDwn

Specifications:

Frequency Range:	155.52 MHz
Available Stability Options:	±100 ppm ±50 ppm ±25 ppm
Input Voltage:	5.0 VDC ± 5% 3.3 VDC
Operating Temperature Range Options:	0 +70°C -20 +70°C -40 +85°C
Storage Temperature:	-55 +125 °C
Aging (PPM/Year) Ta=25C, Vdd=5/3.3V	±5
Output Level:	TTL/CMOS
Packaging:	Tape & Reel Tube (1K / Reel)

Output Clock Switching Characteristics

	TEST CONDITIONS	Min	Typ	Max	Unit
Duty Cycle:					
TTL @ 1.4 V, 4.5–5.5 Vdd	CL = 15 pF	40		60	%
CMOS @ Vdd/2, 4.5–5.5 Vdd	CL = 15 pF	40		60	%
Output Clock Rise/Fall	CL = 15 0.8V–2.0V, 4.5–5.5 Vdd 0.2–0.8Vdd, 3.0–3.6 Vdd			0.9 2.4	ns ns
Start Up Time	From power on			2	ms
Power Down Delay Time	PWR_DWN pin Synchronous Asynchronous		T/2 10	T+10 15	ns ns
Output Disable Time	Synchronous Asynchronous		T/2 10	T+10 15	ns ns
Output Enable Time	OE pin LOW to output Hi-Z T = Freq oscillator period			100	ns
Period Jitter: 1 σ Sigma	> 1,000,000 SAMPLES Peak to Peak > JEDEC std JESD65		8 70	12 100	ps ps

Operating Conditions: min max

Vdd	3.0	5.5 V
Digital Supply Voltage		
CTTL	15	pF
Max Cap Load (TTL)		
CCMOS	15	pF
Max Cap Load (CMOS)		

Electrical Characteristics

Input Characteristics (Pin 1):					
VIL, Low-Level Input Voltage TO DISABLE OUTPUT	4.5–5.5V Vdd 3.0–3.6V Vdd			0.8 0.2Vdd	V V
VIH, High-Level Input Voltage TO ENABLE OUTPUT OR NO CONNECT	4.5–5.5V Vdd 3.0–3.6V Vdd	2.0 0.7Vdd			V V
IIL, Input Low Current	VIN = 0V			10	µA
IiH, Input High Current	VIN = Vdd			5	µA
Output Characteristics:	3.0V–3.6V Vdd, 8 mA IoL			0.40	V
VoL, Low-Level Output	4.5V–5.5V Vdd, 16 mA IoL			0.40	V
VoHTTL, Hi-level Output TTL	4.5V–5.5V Vdd, -16 mA IoL	2.40			V
VoHCMOS, High-level CMOS Voltage	4.5V–5.5V Vdd, -16 mA IoL 3.0V–3.6V Vdd, -8 mA IoL	Vdd-0.4 Vdd-0.4			V V
Power Supply Current: (unloaded)	4.5–5.5 Vdd 3.0–3.6 Vdd			45 25	mA mA
Standby Current:			10	50	µA
Input Pull-Up Resistor	4.5–5.5 Vdd, VIN = 0V 4.5–5.5 Vdd, VIN = 0.7V	1.1 50	3.0 100	8.0 200	MΩ KΩ
CLKOUT Pull-Down Current	5.0 Vdd		20		µA
Output Enable / Power Down Mode	Output is Tri-Stated Controlled by pin 1 input				

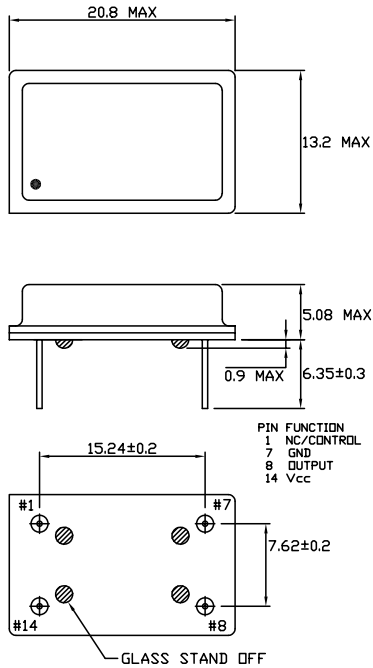


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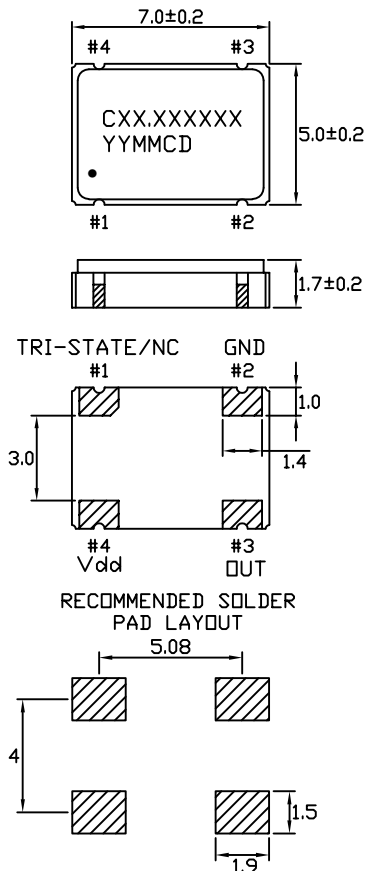
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Note: Bypass Vdd to GND with a 0.01 μ F Capacitor

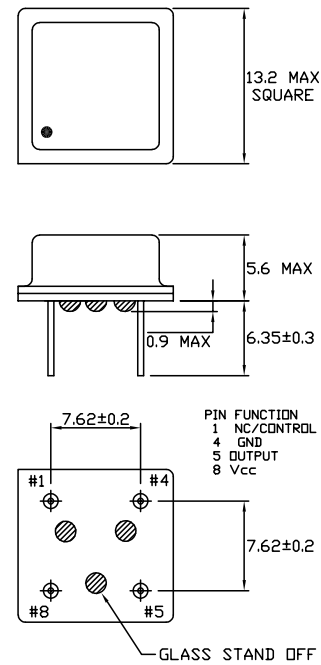
Style 1 Full Size 14 Pin Dip



Style 7 5x7 Ceramic SMD



Style 4 Half Size 8 Pin



Style 8 Plastic SMD

